R16

Code No: 134CF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, December - 2019

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, MCT, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b as sub questions.

PART – A **(25 Marks)**

1.a) What is unit distance code? [2]
b) What are the basic operations in Boolean algebra? [3]
c) Why subtractor ICs not available? [2]
d) What is a priority encoder? [3]
e) What are the basic types of shift registers? [2]
f) What are the various methods used for triggering flip-flops? [3]
g) List the features of sequential circuits. [2]
h) What is a Modulo-N counter? What are the applications of this counter? [3]
i) Explain capabilities of finite state machine. [2]
j) Define Merger graph of n-state machine M. [3]

PART – B **(50 Marks)**

2.a) Covert 105.15_{10} to binary, octal, hexadecimal.
b) What is hamming code? How is the hamming code word tested and corrected. [5+5]

OR

3.a) Simplify the following Boolean expressions using the Boolean theorems.
i) (A+B+C) (B′+C) + (A+D) (A′+C)
ii) (A+B) (A+B′) (A′+B)
b) Why a NAND and NOR gates are known as universal gates? Simulate all the gates. [5+5]

4.a) Simplify the expression $Y=\sum m(7,9,10,11,12,13,14,15)$ using the k-map method.
b) Simplify the following Boolean function $F(A,B,C,D)= \sum m(1,3,7,11,15) + \sum d(0,2,5)$. [5+5]

OR

5.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
b) Realize the function $f(A,B,C,D) = \prod(1,4,6,10,14) + d(0,8,11,15)$ using (i) 16:1 MUX (ii) 8:1 MUX. [5+5]

6.a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.
b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits. [5+5]

OR

7.a) Design, draw and explain a synchronous MOD-12 down-counter using j-k flip-flop.
b) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams. [5+5]

8.a) Explain in detail about serial binary adder with neat logic diagram.
b) Draw a state diagram for the sequential machine whose output is '1' when the sequence is 01. [6+4]

OR

9.a) Discuss about the approaches of designing synchronous sequential finite state machines.
b) Design a 1101 sequence detector and draw its logic diagram. [5+5]

10.a) What are the Moore and Melay machines? Compare them.
b) Explain the procedure for state minimization using the partition technique. [4+6]

OR

11.a) Reduce the following machine shown below.

PS	NS, Z	
	X = 0	X = 1
A	B,0	C,1
B	B,0	A,1
C	A,1	E,0
D	B,1	C,1
E	A,0	D,0

b) Explain concept of minimal cover table. [4+6]

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