R16

Code No: 135AY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, December - 2019
LINEAR AND DIGITAL IC APPLICATIONS
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) List the AC Characteristics of Op-Amp. [2]
b) Significance and definition of upper and lower threshold points of a Schmitt trigger. [3]
c) List out the applications of 555 timer. [2]
d) Why the Reset pin of IC 555 is normally connected to Vcc? [3]
e) Give the principal of weighted resistor type DAC. [2]
f) Define the following terms as related to DAC: [3]
i) Linearity ii) Resolution
g) What is the purpose of priority encoders? [2]
h) Realize NOR gate with CMOS circuit. [3]
i) List the applications of ROM. [2]
j) Differentiate Static RAM and dynamic RAM. [3]

PART – B

(50 Marks)

2.a) Explain significance of virtual ground in an op-amp.
b) An IC op-amp 741 used as an inverting amplifier with a gain of 100. The voltage gain vs frequency characteristics id flat up to 12KHz. Find the maximum peak to peak input signal that can be feed without causing any distortion to the output. [5+5]

OR

3.a) Explain effect of bias current on output voltage.
b) Design a practical integrator circuit with a DC gain of 10, to integrate a square wave of 10KHz. [5+5]

4.a) Draw the schematic diagram of monostable multivibrator using IC 555 timer and explain its operation.
b) How to generate a sawtooth wave form? Explain the working of such a circuit with neat circuit diagram. [5+5]

OR

5.a) For all pass filters, the values of R and C are 7.95K and 0.02μF respectively. If the input frequency is 1.5 KHz, calculate the phase shift.
b) Why is capture range always smaller than the lock in range? Explain. [5+5]

6.a) Draw the circuit of a Weighted Resistor DAC and obtain expression for n-bits.

b) Sketch the diagram and explain the operation of Successive approximation type ADC. [5+5]

OR

7.a) Draw the typical dual slope converter and explain.

b) The logic levels used in an 8-bit R-2R ladder type DAC are logic '1'= +5V and logic'0'=0V. Find the output voltage for an input of 10110111. [5+5]

8.a) Implement the following Boolean expression using 74×151 IC

$F(z) = AB+BC+AC$.

b) Explain in detail about parallel binary adder with neat diagram. [5+5]

OR

9.a) Design a priority encoder.

b) Design full subtractor using gates. [5+5]

10.a) Draw the internal structure of synchronous SRAM and explain the operation.

b) Implement the following Boolean function using ROM: [5+5]

$F_1(A_1, A_0) = \sum m(1,2)$ and $F_2(A_1, A_0) = \sum m(0,1,3)$

OR

11.a) Explain the internal structure of a 128*1 ROM using two dimensional decoding.

b) Briefly explain about Ring counter with block diagram. [5+5]

---ooOoo---