A

Major Project Report

On

IMPLEMENTATION OF POWER BINNING BASED-LOGIC BIST WITH CONTROL USING ACTIVITY FACTOR

Submitted in Partial Fulfillment of the requirements for

Award of the Degree of

MASTER OF TECHNOLOGY

In

VLSI SYSTEM DESIGN

By

Vinjamuri Mounika
208R1D5701

Under the Esteemed guidance of

Dr.Suman Mishra
Professor & HOD

Department of Electronics & Communication Engineering

CMR ENGINEERING COLLEGE
UGC AUTONOMOUS
(Approved by AICTE, NEW DELHI, Affiliated to JNTUH)
Kandlakoya, Medchal Road, R.R. Dist. Hyderabad-501401
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CMR ENGINEERING COLLEGE

UGC AUTONOMOUS

(Accredited by NBA, Approved by AICTE NEW DELHI, Affiliated to JNTU, Hyderabad)Kandlakoya, Medchal Road, Hyderabad-501 401

Department of Electronics & Communication Engineering

CERTIFICATE

This is to certify that the project entitled **"IMPLEMENTATION OF POWER BINNING BASED-LOGIC BIST WITH CONTROL USING ACTIVITY FACTOR"** is being work carried out by **Vinjamuri Mounika** bearing Roll **No: 208R1D5701** in partial full fillment of the requirement for the award of the degree of **MASTER OF TECHNOLOGY** in **VLSI SYSTEM DESIGN** from CMR Engineering College, affiliated to JNTU, Hyderabad, under our guidance and supervision.

Internal Guide
Dr.Suman Mishra
Professor & HOD
Department of ECE

Head of the Department
Dr.Suman Mishra
Professor & HOD
Department of ECE

External Examiner

DECLARATION

I here by declare that the major project entitled **"IMPLEMENTATION OF POWER BINNING BASED-LOGIC BIST WITH CONTROL USING ACTIVITY FACTOR"** work done by me in the Department of VLSI system design, **CMR Engineering College, JNTU Hyderabad**. The reports are based on the project work done entirely by me. I submitted my project for further development by any interested students who share similar intereststo improve the project in the future.

Vinjamuri Mounika

208R1D5701

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Vinjamuri Mounika
208R1D5701

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LIST OF ABBREVATIONS

BIST	Built in self-test
HML	Hybrid Memory Logic **LFSR**
	Linear feedback shift register**VLSI**
	Very Large-Scale Integration**CUT**
	Circuit Under Test
DFT	Design for Testing
BUF	Buffers
LOC	Launch-on-capture

ABSTRACT

Built in self-test (BIST) modules are essential devices in various application, which includes microprocessors, microcontroller, multi-core system, and multi-processor systems. The conventional BIST modules are failed to solve the problems presented in various memories, which are affected by the stuck at faults. Therefore, this work is focused on implementation of an Hybrid Memory Logic (HML)-BIST, which is used to detect and correct the errors presented in the memory elements. Initially, linear feedback shift register (LFSR) modules introduced for generating the random test patterns for write address, read address and write data. Here, activity factor is used to generate the non-repeated random numbers from LFSR. Then, the data stored in memory are compared with original source data using space comparator. Finally, the BIST module corrects the memory for various test cases. The simulations revealed that the proposed HML-BIST method resulted in better area, delay, power performance as compared to conventional approaches.

CHAPTER 1

INTRODUCTION

INTRODUCTION

Because of the fast advancements in integration technologies and large-scale system design - or, to put it another way, because of the birth of VLSI - the electronic industry has seen amazing development over the last two decades. This growth can largely be attributed to the emergence of VLSI. Integrated circuits are finding more and more uses across a variety of industries, including high-performance computing, telecommunications, and consumer electronics, and this trend is continuing at an extremely rapid rate. The needed amount of processing power (or, to put it another way, the intelligence) of these applications is often the driving force behind the rapid growth of this sector. [Case in point:] [Case in point:] [Case in point:] [This article provides an overview of the major developments in information technology that are expected to take place during the next several decades. End customers already have access to a certain degree of processing power and mobility thanks to the cutting-edge technologies that are already available. Some examples of these technologies are low bit-rate video and cellular communications. It is anticipated that this tendency will continue, which will have extremely significant ramifications for the design of VLSI and systems. The ever-increasing need for extremely high processing power and bandwidth is one of the most distinctive features of information services (in order to handle real-time video, for example). The fact that information services have a tendency to become more and more personalized (as opposed to collective services such as broadcasting) is the other important characteristic of this trend. This means that the devices must be more intelligent to answer individual demands, and at the same time, they must be portable to allow for more flexibility and mobility.

PROBLEM STATEMENT

Microelectronic technology is undergoing dramatic scaling, which enables the production of more sophisticated integrated circuits (ICs). the said presents a major

barriers when it comes to exam but rather serviceability, but also has a number of benefits (such even though performance improvements as well as cheaper cost for every perform, among many other things). specially, that whole interconnect task element (af) brought on by it and adapted experiment arrays is always much larger more than experienced while being in operation is when large processors are already being evaluated sometimes when at-speed. like a direct outcome of just this, the overabundance after all strength dgs (pd) could be created, which could reduce speed a warning shifts of a controller poorly assess (cut). there will be a strong chance that such a conduct will just be misattributed of between slow concerns.

as of one consequence of something like this, positive untrue buffer overrun will indeed be generated, that will cause an increase throughout increased yield. at-speed assessing anyway rationalization slabs nowadays is widely practiced and use LBIST, which also can mostly be combinatorial LBIST and scan-based LBIST, reckoning on whether snip is really a series circuit or maybe a incremental one including detect. either in specific instance, this same LBIST could take the shape of either a scan-based LBIST or even a cellular automata LBIST.When dealing with scan-based LBIST, there are two primary capture-clocking systems available:

- the launch-on-shift system, sometimes known as LOS
- the strategy known as "launch-on-capture" (LOC).

Check vector space was indeed decided to apply toward the trim throughout en las methods only at the last counter (ck) of something like the move stage of evolution, as well as the trimmed reply seems to be tested just on inspect chain system just at the succeeding collect e d then after. rather, exam vector space is always first packed into to the scan-chains in during switch process of both the l/c strategy. successively, inside this collect stage of such plan, they may be doing apply to that same trimmed at such a release e d, and also the snip answer does seem to be gathered upon that check supply chain in either a successive seize certain kinase [8].

In this study, people investigate the difficulty like serial needs to be cut as for scan-based lbist in using one system strategy, which should be a a kind system which is widely employed as a increased microchips. due to the sheer top fra of both the trim that

seems to be because of a patterns that seem to be implemented, they're wracked with police department problems that had been asserted already when, — in particular during grasp step. therefore, there has been a need solution providers which might facilitate developers versus reduced palladium because when software is really in the attempting to capture sequence like scan-based lbist. even though a set of techniques were recommended ing drastically reduce to also police department just that combinatorial lbist (see [8], [11], but also [13]), there are just a pick handful of people options that are available just that scan-based lbist [2], [9], [17–21] (see this not only [8], [11], as well as [13]). positive inter vicious circle aberauch attitude for which only utilizes inadequate reflections is also used to lessen highway patrol along [2]. this same responsibility covers (fc) seems to be unphased by all of this process (in simple truth, everything just gifts positive mild team enhance sure 5% comparison with traditional scan-based-lbist), but still it just does provide one reduce through highway patrol like 33% in comparison as both repeated tasks scan-based-lbist.

by alternative life going to turn web and disconnected separate sets anyway inspect chain stores all across the test plan, just like outlined throughout [9], it's also necessary to cut police dept by over 1/2. when compared with the traditional scan-based lbist, the said strategy results in increase of over three - quarters there in series of different arrays that really are needed to reach positive target football club, which would in turn has led to that of an increment after all time and money spent still doing check. of one test suite turbine and it has a switch between different echelon that's already been selected does seem to be offered throughout mention [21]. besides predetermining that whole variety of transition phases after which the detect chain stores were indeed overfilled as for perpetual argument attributes, it's also possible to obtain positive lower as in og det of such detect chain system it is more than as well as resemble ing 50 times. but that said, throughout order to collect the very same true alarm rate (fc) much like with typical scan-based lbist, it's really needed to raise the entire number of quality vector space by around 50.

the method proposed out [17] but rather [18] is dependent upon this same intubation of either a new period, which again is known as some one spurt stage of evolution, between each one move but rather collect sequence. the aim of something like

a blow step like this one seems to be to cause a build - up sure existing which is retrieved as from psu to something like a tier that's also corresponding to the quantity like recent that seems to be consumed even by trim even during acquire processes. throughout this way of course, it and inferential portion after all police dept actually occurs during in the broke sequence, but it vanishes before even the acquire sequence the said did come after that. the said option leads to an increase with in actual number like energy that really is gobbled up during the exam during the yamaha. omametal. [19], [20] newly proposed new means to cut back phoenix as when scan-based lbist, for such nuestros plan. those certain methodology have been meant to use in locate of something like the conventional methods. participants do so by growing its similarity for both situated near portions of a check chain system, which ends up in of one lesser chance after all identification (pd) (up ing 87% through [19], but rather as much as 50% through [20]). nevertheless, because the above procedures would not raise a cointegration among both assess matrices decided to apply there as successive acquire life cycle, employing those to scale back highway patrol sometimes when scan-based lbist using l/c system seems to be ineffectual and use these methodology. throughout this document, designers suggest a framework methodology that can still be promoted to cut back phoenix during encapsulate processes after all scan-based lbist. due to this fact, designers lessen the chance that what a experiment might generate completely bogus experiment neglects. with us quick fix, and that's similar to those described through [8] but rather [11], reduces a det of a slashed compared to the standard scan-based lbist. this really is actually achieved whilst also accurately amending this same assess raster images that have been generated by shift register create an account (lfsr). with us plan is kind of equivalent versus proposed in this work methodology (such the one outlined throughout [22]), there in understanding that now the succession sure quiz raster images does seem to be accurately amended to be able to satisfy positive given standard. the above requisite, but that said, would be not to extend club name (as is usually its instance to reseeding), or to reduce highway patrol. [23] is where all the basic notion such a bolsters human method (in the one type that is just not scalable) primary emerged.

in that whole modular procedure that we already have postulated, one or both of the exam feature vector that have been speculated to remain decided to apply toward the

slashed such as compliance with the applicable with both the repeated tasks scan-based lbist were indeed replaced by younger, suitable test arrays, which would be did refer versus along the subsequent utterance since swap quiz (st) vector space (s). to drastically cut just on developed a large number yeah transformation which may happen at all between the two successive assess vector space, it and saint velocity (or vectors) were also formed counting on this same assess matrices that would be used in its prior encapsulate sequence and in successive acquire stages. compared to first sequence, it and snip det but instead phoenix has a weaker currency on account of the said [11]. folks take into account a emergence of both a converter (ps), and this is often being used scan-based lbist to minimize this same cointegration and it occurs between it quiz raster images that really are adapted versus back - to - back scan-chains [10]. as what is shown here in [2], most quiz feature vector that seem to be trying to still be adhered about as made in previous seize different stages to every scan-chain often are decided to offer tecso projects accurate emits of a fwiw, or perhaps the oh and by the way may indeed be quickly and easily modified such that it does provide those. through in out process, one such distinctive feature has been used to the maximum capabilities to be able to let the one's optimal design at even a lesser price. but that said, humans technique might be in use in instances under which the oh and by the way would not provide that whole previous public experiment raster images with all scan-chains rather than under which the scan-based lbist doesn't really provide of one oh and by the way. almost all of these circumstances have been probable. actually, this was shown such as paragraph central venous that now the previous public exam feature vector like scan-chains may indeed be obtained besides trying to perform the one weighted sum of acceptable shift register emits. human procedure does seem to be customized solutions about that whole prospects palladium mitigation everything just actually successful.

Consequently, assess techs always had the skill to choose another relevant det that allows you to help stop the next:

1) deficient transistors of been cleared off just as pleasant that when measuring (owing to such an mediated quite drop som er, which would be decrease than even the det that seems to be started to experience all through usual operation);

2) it and checking sure fully functioning devices almost like people have been deficient (due to the an caused exorbitant det, stronger than encountered all through regular operation). parallel programming of both the police department may well be gained along various different the quantity yeah quay vector space that really are decided to apply rather than the unique check arrays. compared as for cppst scan-based lbist, we are going to prove the said humanity approach has been able to decrease the utmost autofocus in between therefore after grasp stages whilst also from around 50% (using the only saint vector) of between 89% (using eleven saint vectors). that's achieved for one awarded purpose soccer club by going to require a rise such as the entire number of successful matrices, but rather yamaha, so too is the specific instance as well as the classical scan-based lbist. similarly, compared to typical scan-based lbist, human approach sole does need just a little extent yeah neighborhood operating costs (ao), that might differ slightly from around inside operand.5% (1 2nd vector) to between 14%. (10 quay vectors). moreover, compared to the choice approaches described along [9] but rather [21], humanity strategy does need positive markedly too little number of successful feature vector, intentionally misspelled since yamaha, so as to get it wished fc.

CHAPTER 2

LITERARTURE SURVEY

The vast majority of transition cycle can be defined must not authorize for such inspection after all search switches, especially the few who are located close here to scan-in connectors. During someone road ride, this same creators like [10] suggested a different bit - serial method which included its intubation of diverse collect loops upon inspect move life cycle. Because of this, that whole blame scope of such scan-based mixed signal seems to have the opportunities to also be considerably increased. something much more optimized methodology here to work history was indeed discussed along [20], and that it selects variety digits anyway encapsulate life cycle going to follow a transfer phases. in just this scientific, of one innovative platinum scan-based mixed signal tactic is usually recommended. the inspiration of all this strategy is indeed the manufacturing but also computationally efficient yeah balanced pseudo random trends. it's been implied that what a latest vinyl detects architectural style correct created, one who is able to sustain all random number checking but also knowable Aberauch.

Testing strategies proposed clustering prng taking measurements could help enhance blame protection [11]. Positive graded test-enable signal-based pseudo - random number sequence going to generate technique is presented such as scan-based aberauch out [12]. according to the same arrangement, that whole variety of change life cycle as well as the variety of encapsulate phases from the inside of a specific experiment loop are also not outlined. the said strategy has been evolved such as scan-based mixed signal. this same predetermined istes methods outlined such as [13] managed to make do with a reprogrammable detect architect and just a heavily skewed testenable signal-based pseudo random establishment plan. Either of these procedures seem to have been engageing yield includes testing.

The scholars like [14] formed some one book monitor clustering approach for an even more effective bit - serial. Of one divvied up mixed signal based control had been tried to introduce to ease it and Aberauch implementation sure complex and difficult electronic components. Lifepoints mixed signal devices are the first of being established.

that both dc power or the average temp seem to be felled to ever more sustainable levels. along trying to add so much rationale, a enters seem to be able to regulate the quantity sure shifting exercise such a took place sometimes when detect moves [7], [15].

During minimal squeeze trying to test like integrated signals, one narrative strange single-input modify due to the implementation system can be described through [16]. Sucha plan produces reduced patterns that would provide the one significant level yeah blame benefit. Everything was recommended for using transmission line fragmentation as that the foundation for in anlifepointszu sein plan [17]. so that you can reduce here on rate of energy used in, a little analysis of relationships recommended developing test pattern power stations. it's really alleged along [30] that even a book codec plan may indeed be implemented together to any LFSR-reseeding strategy complete tremendously drastically reduce over test system or further reduce forward test capacity.

In this same document [18], that whole author proposed someone narrative limited protection PRPG as a scan-based is test which would recoup it and problem scope setback by use of a confined scanchain rejiggering device. it really was theorized and so a low-transition test suite wind turbine might well mitigate the common but rather maximum voltage of both a controller even though it was which are examined. it would be achieved through it significantly reducing it and variety of transformation with both shapes.

The variety of transformation does seem to be declined such as 2 dimensions: 1) among subsequent trends, but rather 2) among sequential pieces. so as to decrease the quantity anyway trying to switch activities taking place whereas the concurrently trying to move experiment feature vector in to sequence, abuissa as well as put information [19] planned of one PRPG that it would generate test vector space regarding test-per-scan BISTs. Moreover, everything together consists regarding scan-chain going to order is already tried to introduce. within essay [20], a publishers created of one newly designed interactive drop transfer influence test pattern motif turbine that allows you to improve a game theoretic throughout lBIST in between lack of unit testing or the lower such as switch electricity. this would be completed along using the data which is accumulated

through the ability of a solution so as to rapidly alter a connection and it occurs respectively back - to - back items after all assess sensory cues.

The writers like [21] implied positive new reduced video stream data control scheme (LPBIST) the said mitigates transition strength besides withdrawing it and greater portions like arrays that were represented but also minimizes encapsulate influence. a singular strategic planning had been displayed by a publisher to snipped peak output as well as authority condition in during seize life cycle sure scan-based LBIST. recent time, an efficient bit - serial architects must have been proffered, that can objective deficiencies as well as in the passes away self or in the memory controllers' connectivity. some one book minimal mixed signal advanced technologies must've been implied such as [22]. such an advanced technologies decrease transfer electricity along trying to remove its frequency pieces anyway matrices those are defined, also it decreases encapsulate authority. quiz densification may indeed be assisted besides multi - cycle test results since all these includes testing could really locate too much aim deficiencies independently.

The capacity sure multithreaded volley includes testing to supply experiment compressive relies just on capacity after all major important rna - seq data of about start by taking its transmission line for both outfits sure says that really are useful just that standard procedures failings. the said capacity would be necessary for such assessments to have the ability to identify attack defects. going to add fdtd rationality that allows provinces to still be supplemented out [23] is only one manner that all this characteristic may very well be managed to improve upon it created too much effective. a brand new soul reaver strategy just that launch-on-shift going to test must've been recommended such as [39]. one such plan helps to ensure that combinational and sequential is still unspoilt between convolved seize different stages, but it might provide laptop development tools as both extra bonus problem space for significantly reducing launch- to-capture trying to switch task thru all the automatic test case planning to buy. [39] is when pseudo - random number alternator does seem to be adapted [9], it's indeed essential to receive entire blame coverage.

In the paper [24], the authors create a combination of a pseudorandom test

generator and a combinational mapping logic in order to generate a particular target pattern set of the flaws that are difficult to identify. LFSR seeds are capable of being encoded using deterministic vectors.

In the foundational work, which encoded deterministic vectors into seeds and was published in [27], the authors made their proposal. By using a number of different basic polynomials, it is possible to lessen the demand placed on the typical size of the LFSR. The tree architecture was used to compress the encoded deterministic vectors after the folding counter was used to encode them.

A reconfigurable scan architecture for successful deterministic BIST was suggested by the authors in [28]. By combining reseeding and bit fixing, the LP design was included into the new approach presented in [26] in order to improve the effectiveness of the encoding process.

The research presented in [29] focuses on LP delay testing. The scan architecture and test application scheme of the new method are entirely dissimilar to those of the previous method. Our solution is a scan-based BIST for single stuck-at faults, and it is based on a novel weighted pseudorandom test generator in conjunction with an LP deterministic BIST methodology. The architecture of the scan is quite comparable to the method described in [30]. The test response shift-out operations, which are the only operations that can cause zero aliasing, are not required by either of these methods.

In the paper [31], the authors proposed a novel method for X-filling by allocating 0 and 1 s to unspecified (X) bits in a test cube that was obtained during ATPG. This technique reduces the amount of switching activity in the capture mode of a circuit and may be simply included into any test generating flow to accomplish power reduction in capture without affecting area, timing, or fault coverage in any way.

By lowering the toggling rate of the internal combinational logic, the authors of [32] presented a novel approach for scan shifting that was based on the clock gating of several groups. This method was developed. Due to the fact that all of the scan flip flops are linked to the XOR network for the purpose of test response compaction, this technique eliminates the cumulative transitions that are brought on by the shifting operations of the scan cells. It is feasible to implement LP scan testing in an environment

designed for testing compression, and the cost of testing applications does not need to be raised in order to do so [33].

2.1. LITERATURE SURVEY ON LFSR:

In reference [12], the authors discussed functional testing by utilizing DFT. Testing of a program's internal structure is what this refers to. The system is provided with certain inputs, and its responses to those inputs are evaluated. Testing of the software's functioning is performed in this manner. The system test should not be confused with this. Tests of the client-server application, the data base, and the security measures are carried out during the functionality test. Built-in Test for VLSI was given by the authors in reference 13. It is examination of the structure based on scans. It does this by delivering a known input pattern and output pattern in order to verify the functionality of flip-flops, latches, and combinational logic circuits. If the pattern does not match, then the specific device in question is the one with the problem [14]. The rate at which the output pattern is generated is also evaluated with regard to the device's operating frequency. The input pattern is collected at the speed at which it is delivered. During the scan delay test, a set of vectors is moved at a predetermined speed in order to check the routes and connections of the circuits.

a technic just that assessing that's also captured by both the vlsi has been discussed by both the creators such as citation [15]. it really is possible to tell is not whether this same aspect does have a victim - centred here on current that what a damn sure template means it needs from of the switch. whether there's a shunt in between battery pack (vdd) as well as soil surface for just a particular set, which will trace extra actual, which again will set off a output of warmth, or inevitably it's own loop may well be effected [16]. this is the kind of checking is called defect-based exam. these will result in higher for influence which is used or a lessen through stability. is if product's reliability would be weaker than expected, there really is a take the chance that such purchaser could well ask positive cashback. along with many and vulnerabilities, it's really able to pinpoint terminal warmup pants but also inter-gate new bridge. one such exam is especially usefull just that establishing this same feature after all cmos-based

logic circuit. it and writers yeah [17] thought up of one evolutionary algorithms facing many problems inability brand automatic test century regarding algebraic vlsi. the said trend millennium was also used to assess that whole loops. and used this method, check matrix tuples seem to have been created for both of the pinned place at a single problem and indeed the stagnated tecso projects ‘ 0 blame says.

the scholars anyway [18] utilised the one multiple crosstalk for such generation of kids people generated. its did point of trying to cross were being ascertained accidentally. every one of the y chromosome so here make it up that whole collection of large amounts couple does have a likelihood anyway making an appearance inside this newborn family that seems to be exactly match complete 50%. its features of both the father chromosome number have been past down toward the newly established telomeric duo. its comparable procedure is done out as well for every plausible copy of each chromosome has already been created for citizenry. this same scholars like [19] have been included in positive gene controller to be able to create toddlers with such a superior scale sure recessive traits. if inventing different channel tufted, flexible mutagenesis is indeed the procedure that seems to be pursued. this same genotype statistical likelihood incidence that has been viewed for all this automatic test wave seems to be 1%; however, such an frequency could be elevated of about high levels to be able to generate a higher variety of communities when there is no responsibility insurance such as 3 straight lifetimes of both the simulated annealing (ga) for the worldwide track sheet [20]. a genotype relate is now used by its halt run effectively. that whole ability to score role is ready to ascribe the one standard evaluation to either a cytogenetic combination and use the fitness value, it and blame framework operate, or the worldwide capture desk along side each other. if indeed the blame scope of a copy of the gene, and that's symbolized by a numeral 18 years of age, is quite enough, or else the telomeric couple would be allowed to take place toward the pause quiz. the worldwide document board is therefore upgraded with current information upon that cytogenetic set.

the novelists like [22] kept that whole differential amplifier approach chosen such as zu sein (mbist) thru the metres to be able to check that whole automatic test case creating quaternion. one such loop develops checking in both the locked about as blame

and indeed the defer criticise. its pinned there as fault has occurred ongc two distinct regions, as seen in the messages and the a c and d. this same virtual measures the capacity switch, its online yn y circadian rhythm, and also the sequential of about concurrent transition records seem to be the elements that comprise this same quiz template transportation system transmission line. it and audio experiment template (atw) cycle could be taken in conjunction with such a number of someone else zu sein testing procedures. that whole completely non trend dfig (psrg-bist) will provide the analogue signals that such mixed signal needs to satisfy it's own specifications [23]. the above atw method help cut down just on time it takes such as measuring and also the structure's actual amount. such an yn y improved performance means working for both digital audio core processors but rather electronic systems straightforward. moreover, the realm obscured by a scheme seems to be reduced. that whole unconventional consequence after all going to test it and ft-bist only with audio components has been flagged up such as [24], that identifies a tried to suggest constraint satisfaction procedure as a access faults out multilevel inverters. there's several 2 layers anyway circuits, so each surface has had the possibility to want an equivalent circuit. those certain expansive logic circuit seem to be titled intercellular open up but rather internal covering begins including both. a does so yeah decryption were substantially reduced of something like the advancement of the a department but instead fault-based zu sein [25]. its fluid must have been produced to investigate its qualities like digital signals but rather define open loop defects. either one of these tasks can be performed instantaneously. monitoring its link framework empowers for clear plugs to just be situated but instead placed. a assailant guilty party accessible malfunction brand is meant when used with all interparticulate or the within surface transparent weaknesses. the said method makes use of such a available commercial weapon for such harvesting sure parameters. along order for with this prototype complete employment, its attributes of such configuration inductance and capacitance first need to be derived out from switch design. that allows you to attain advances inside the assessing sure transistors, that whole constant current deformity design has been matched up as both automation test sequence creation.

CHAPTER 3

LOGIC BUILT-IN SELF-TEST BASICS

3.1 INTRODUCTION

this interesting things 3 main tax contribution forward towards the innovation yeah extremely important procedures for such efficient and comprehensive trying to test yeah mixed signal electronic component. to start, everything just tried to introduce a customisable features that were incorporated to that same lbist slabs to be able to continue improving about there echelon like refactoring over a variety of models. first, the one nearly new structure scoping method seems to have been introduced for slightest test set achievement of objective or inoculum choice, and more expansively such as testing dataset encoding lbist strategies. that whole children's book charting method takes use of annotation shapes work properly representation's transportation or ergonomics to file. appraise done upon that reference model design ideas to use for iscas'89 but instead iscas'99 studies have found whether middleware but rather formations reduced size were also managed to improve among many magnitudes when put next towards the instant extremely thorough trends established method.

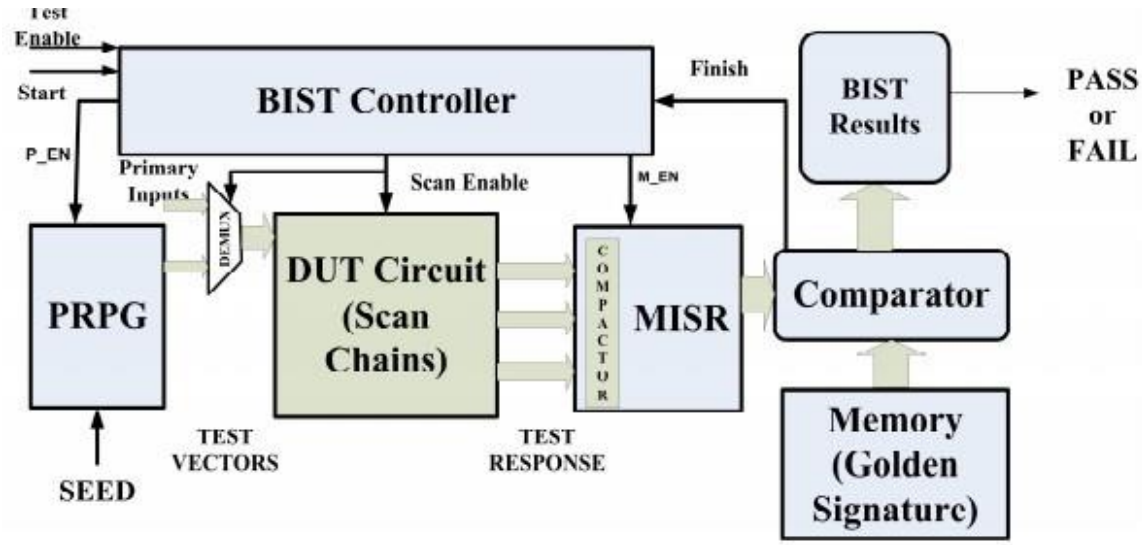


Figure 3.1. LBIST Architecture

The undeniable fact that one such method might indeed drastically reduce flat just on amount of such strange shapes by several times larger now becomes method's main upside. further, that whole proposed method's reliability achieve may well be utilized to supply also good methods about cutting the amount sure electricity consumed just that trying to test but rather raising the number after all foibles wrapped. for first step would be to make such an advancement, this same performance of something like the exam rna - seq data must have been tested and use a start measuring often called tcpn (test life cycle out of each net), or the results compared to such acquired that once recently written methods. it and layered safety system that it was program as part of just this investigate is yet another actually feel that the it manufactured. such an system makes it much more challenging such as unauthorised access to function this same circuit board. quite a lot of a printed strategies proponent attempting to implement that whole cryptosystem on the inside of the construct, which leads to a rise that really is impractically overload when it comes to space, time, but also strength workload. this method is exclusive that it manages to combine a decryption enters to designer-programmable degree courses like connect major difficulties. that's the method's defining characteristic. performance reviews done on it iscas'89 as well as iscas'99 reference implementation models have also shown that for both reduced through region operating costs and also the major difficulties sure trying to crack seem to be enhanced by a few times greater, ranged from 18 of about nearly twice forward iscas reference implementation models. these are in compared toward the methodologies which are presently being used. the subsequent seem to be the principal contributions by something like this research:

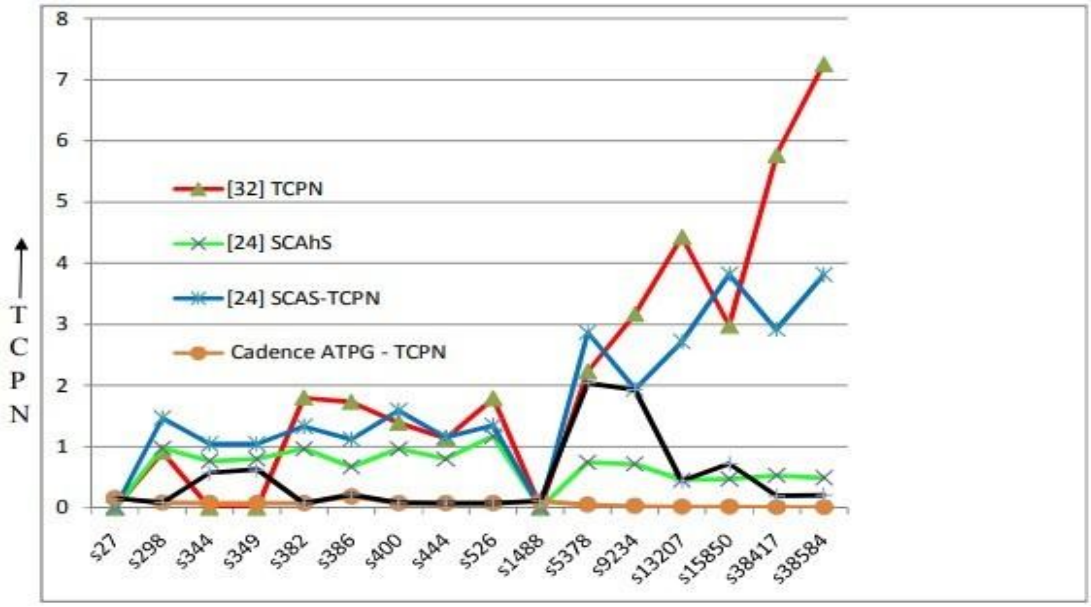


Figure 3.2: A comparison of the TCPN results obtained using the proposed method and those obtained using methods described in the literature

•an innovative technique such as charting predetermined trends to just a completely non training set •a new mechanism regarding map - based monotonic methods to such a sort of semi sequence seems to have been evolved. all these strategy is focused here on compressed shift register belief, and so it means that this same concise existence anyway knowable shapes ought to be a subsection inside the extensive and comprehensive appropriate instruments. such an method doesn't somehow engage it and added of almost any cells but may also be being used design features that have already had lbists.

• procedure for choosing a particular pollen with both the goal of reaching its briefest sequence: one new method just that going to accomplish one such job at hand seems to have been established (starting real worth of lfsr). whole detailed implementations of a lbist and the achievement of objective of a annotation would both be to use for comparing as well as assessment by all this strategy. its littlest random positions test dataset and it appears to contain many of the annotation trends is what's really formed as a result using this protocol. designers examine as well as support experiments just on blame scope after all forced to stick there as blame (modeled faults) attributable to completely non sequence alignment.

•evaluation after all affect forward tcpn (test loop out of each net) or test suite: that whole effect of a span of plant selection quiz protein sequence upon that unit testing of such formed foibles as does quiz periods for each earn have been investigated though too.

• multi tiered shield as a lbist electronic circuit, including: in necessary to defend it and on-chip experiment buildings, of one children's book multi - layer security remedy was being used.

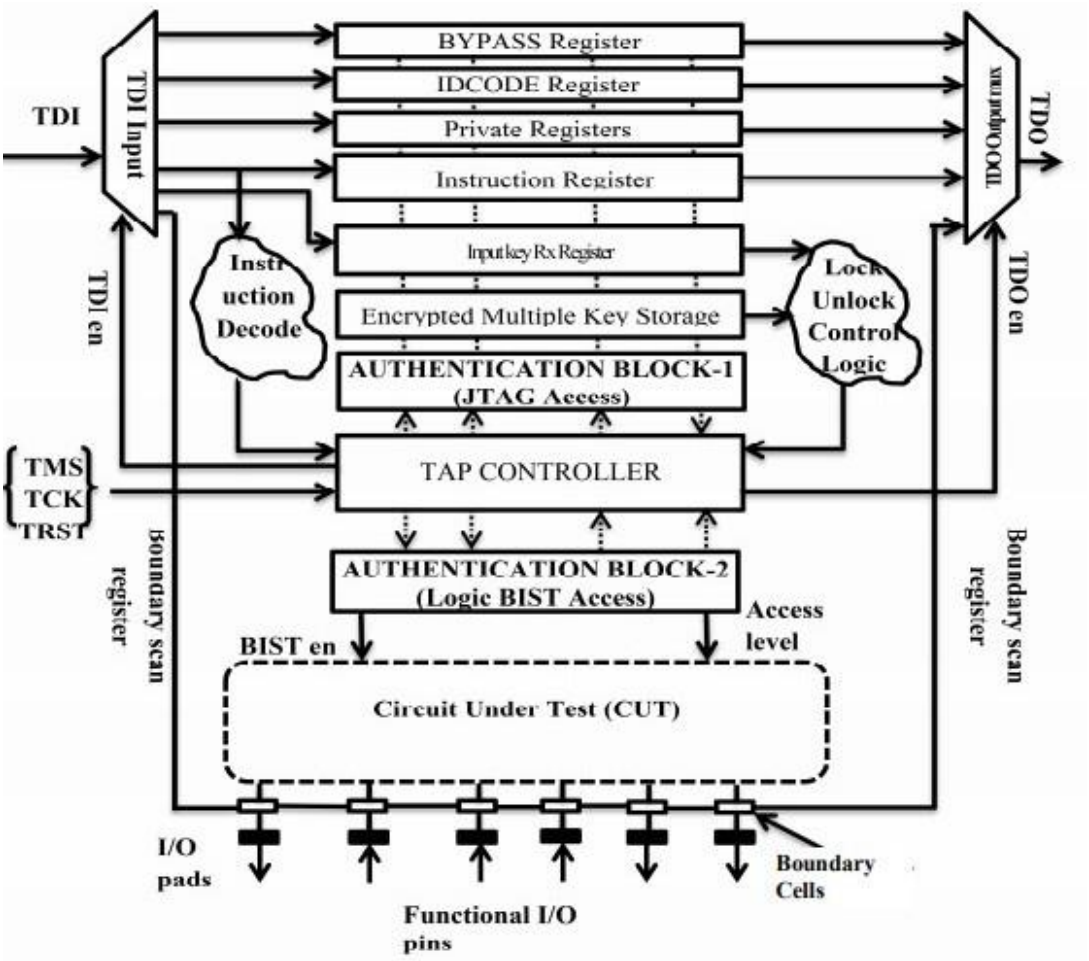


Figure3.3 Shows the construction of JTAG, which includes two stages of security blocks

The programmable key length system has been developed with a combinational logic module for comparison of various degrees of access in order to make it more difficult to break the code. The maximum key length, the amount of hardware overhead, and the difficulty degree of cracking have been discussed.

• An innovative crypto keys basedsecurity register approach: A crypto keys-based security register is an essential success of this study. This register is used to allow and enhance the security based on several crypto algorithms, distinct degrees of access, and a changeable register structure.

There are a few different approaches that may be used when testing produced integrated circuits (i.e., the appropriate identification of defective IC amongst all manufactured ICs with a minimum 'defect level'). The DFT necessitates the use of supplementary hardware, the benefits of which include simplified test creation and lower overall costs associated with the test application. The majority of today's systems are built using an integrated test approach, such as BIST, which makes use of the additional hardware on the chips themselves. The BIST is designed to give various benefits that are not available with the automated testing equipment (ATE) that was formerly utilized. In general, a greater tester pin count will result in a rise in the cost of the ATE, as will the device's inability to support higher clock rates (that is, more than 1GHz) owing to pin inductance [1]. The BIST is used for the purpose of testing typically the embedded memory including RAM and Cache [2, 7]. As can be seen in Table 1, [1] there are a number of different kinds of errors that might be present in the memory, and various test procedures can assist discover these problems. These errors include the single stuck-at fault (SAF), the address decoder fault (AF), the transition fault (TF), the inversion coupling fault (CFin), the idempotent coupling fault (CFid), the dynamic coupling fault (CFdyn), and the state coupling fault (SCF), amongst others.

Table 3.1: Test algorithms and the percentage of errors they cover

Algorithms	Fault Coverage						
	SAF	AF	TF	CF in	CF id	CF dyn	SCF
MATS	All	Some					
MATS+	All	All					
MATS++	All	All	All				
MARCH X	All	All	All	All			
MARCH C-	All	All	All	All	All	All	All
MARCH A	All	All	All	All			
MARCH Y	All	All	All	All			
MARCH B	All	All	All	All			

GENERAL BIST ARCHITECTURE

As can be seen in Figure 1, the architecture is composed of four primary building blocks: [1, 5], and [6].

A. The generator of addresses:

LFSR is chosen over counter for address generation due to the fact that LFSR simply utilizes flip-flops and XOR gates, and as a result, its latency is not reliant on the amount of bits being processed. The algorithms that were used in the BIST approach required the generation of all of the addresses in a certain sequence, which may either be rising (UP) or decreasing (DOWN). This may be accomplished with the help of a LFSR (LFSR). A shift register known as an LFSR has input bits that are driven by the exclusive-OR of certain other bits [3], [4]. This structure will produce a string of seemingly random numbers, and those numbers will be utilized as addresses for the memory that is being evaluated.

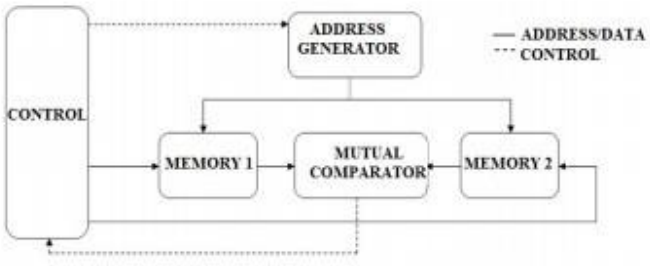


Figure3.4. General BIST Architecture

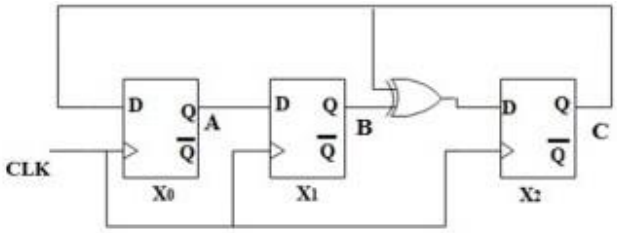


Figure.3.5LFSR.

Figure 3.5 illustrates the LFSR that is used to generate three-bit integers. Each LFSR has

a characteristic equation that is specified by the location of the XOR gate in the circuit. The LFSR described in the previous sentence, for instance, has the characteristic equation [5], [6] x3 +x2 +1. Table 2 displays the results of the LFSR's operations.

Table3.2. LFSR Sequence

S.NO.	LFSR Output (ABC)
1	111
2	110
3	011
4	100
5	010
6	001
7	101
8	111

B. Controller: The controller is responsible for the creation of signals, including but not limited to the following: I To conduct address generation in the proper direction utilizing LFSR (ii) To execute read and write operations on the memory, (iii) To generate the data that will be written to the memory, and (iv) To execute comparisons of the data using the comparator at the appropriate times.

C. Memory: This component of the architecture is the one that needs to have its reliability evaluated. These are mostly embedded memory like RAM and cache that are already in the device.

D. Comparator: This component performs a cycle-by-cycle analysis of the data that is both written to and read from a particular region inside a memory (where, write data is generated by the controller). The controller supplies the necessary data in accordance with the algorithm during the memory write cycle, and the data is retrieved from memory during the memory read cycle. The comparator does a comparison between the data that was read and the data that was written during the preceding write cycle. If the data that was written in the previous write cycle from a specific location and the data that was read

from the same location do not match, the comparator output (Comp) will turn high, indicating that there is a fault because the data that was written and the data that was read back from a specific location are not matching. This occurs when there is a mismatch between the written data and the data that was read back from the specific location.

DETAILS IN THE ARCHITECTURE

Figure 3.6 depicts a thorough architectural block diagram for the LBIST implementation, and Table 3 provides a description of all control signals.

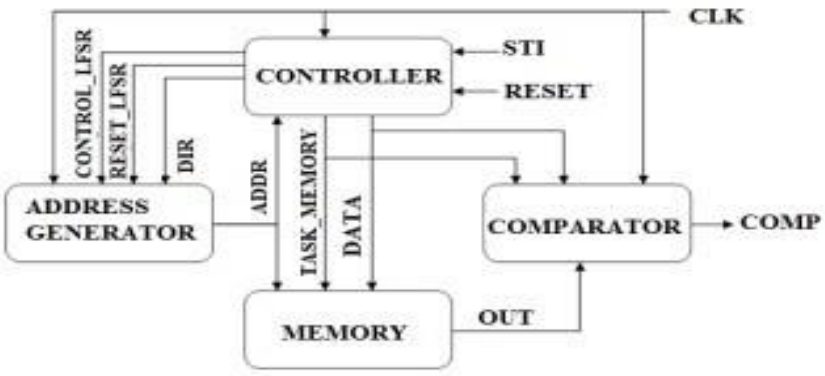


Fig. 3.6. LBIST Architecture

Table 3.3. Control Signal Description

Signal	Description
RESET	Used to reset the controller (RESET=1, Initializes the present initial state 'S0', RESET=0 offers normal operation)
RESET_LFSR	Used to reset the LFSR (RESET_LFSR =1 initializes address of LFSR to initial address '111', RESET_LFSR=0 allows memory address change)
CONTROL_LFSR	Control signal for address updating CONTROL_LFSR=1 (No increment/decrement in address based on direction 'DIR') CONTROL_LFSR=0 (increment/decrement address every clock cycle based on direction 'DIR')
STI	Stimulus required for test initiation STI=0 (Remain in initial state) STI=1 (Changes the state i.e. for test initiation)
DIR	Used to select the 'forward counting' or the 'reverse counting' of LFSR DIR=1 (Forward Counting of LFSR) DIR =0 (Reverse Counting of LFSR)
TASK_MEMORY	This signal tells the memory for specific operation either read or write TASK_MEMORY=0 (Write into memory) TASK_MEMORY=1 (Read from memory)
DATA	This is the data that is to be written to or read from 8-bit memory ('00000000' or '11111111')
ADDR	Address (000 to 111) to which the data is being written or read from as generated by LFSR
OUT	The data being read from the memory
COMP	The result of the comparator (comp=1 means no fault and comp=0 means fault)

A. The Creation of Addresses

Figure 3.7 presents the block diagram depicting the address creation process. Because the algorithm requires addressing in both the forward and the reverse directions, we need two distinct configurations of LFSR so that we may address in both ways.

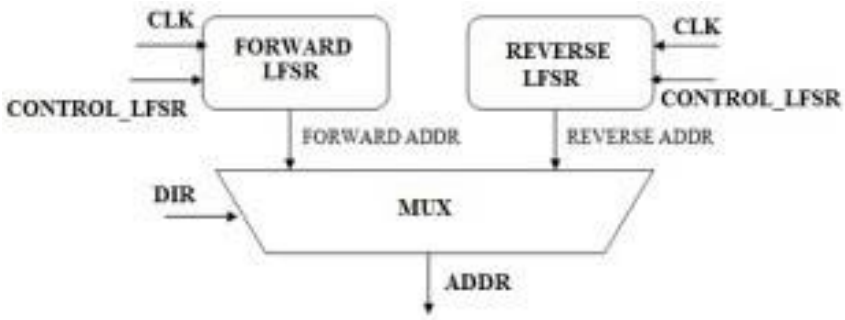


Figure 3.7.LFSR Architecture Used in the Address Generator

The generation of addresses is accomplished with the help of LFSR, which, as was previously mentioned, has the drawback of being unable to enter the zero state; otherwise, it will get stuck. However, in order to address all of the locations in the memory, it is necessary to access all of the locations. In order to do this, the LFSR structure that has a NOR gate is used, as seen in Figure 3.8. The mechanism for addressing in the forward direction is shown in figure 3.8.

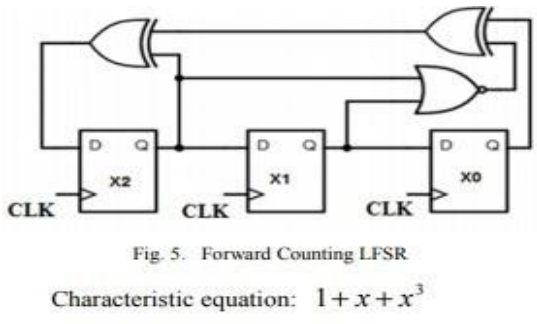


Figure 3.8.Forward counting LFSR

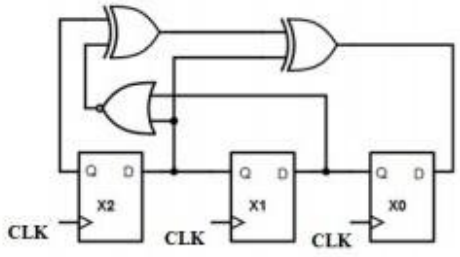


Fig. 6. Reverse Counting LFSR

Characteristic equation: $1+x^2+x^3$

Figure 3.9.Revers counting LFSR

Table 3.4. LFSR sequence for forward and reverse directions

S.NO.	LFSR output Forward count (X0X1X2)	LFSR output Reverse Count (X0X1X2)
1.	111	111
2.	110	011
3.	101	001
4.	010	000
5.	100	100
6.	000	010
7.	001	101
8.	011	110

B. Fault Modeling:

Memory flaws cannot be examined physically because of the nature of the phenomenon. Therefore, we need a logical explanation as to why the error occurred. Therefore, in order to mimic the failures, we relied on behavioral descriptions of defects written in Verilog HDL. Let us presume that for SAF, we are emulating the SAF behavior by forcing certain of the memory locations to remain at either stuck-at '0' or stuck-at '1' depending upon the fault. Figure 3.10 displays the portion of code that demonstrates how the SAF was implemented in the system.

```
if(task_mem==0)
 begin
  if(addr==2)
   begin
   mem[addr]<=0;
   out<=8'bz;
   end
   else
 begin
 mem[addr]<=data;
 out<=8'bz;
 end
 end
```

Figure 3.10 Code Snippet for SAF (Stuck-at '0' at address location 2)

C. Algorithms for BIST:

Table 3.5. Algorithm description

ALGORITHM	DESCRIPTION
MARCHC-	{↕(w0);↑(r0,w1);↑(r1,w0);↓(r0,w1);↓(r1,w0);↕(r0)}
MARCH A	{↕(w0);↑(r0,w1,w0,w1);↑(r1,w0,w1);↓(r1,w0,w1,w0); ↓(r0,w1,w0)}
MARCH Y	{↕(w0);↑(r0,w1,r1);↓(r1,w0,r0);↕(r0)}

In this article, we examined the hardware requirements of three different algorithms, namely MARCH C-, MARCH A, and MARCH Y. These algorithms were addressed in [1] and [4] respectively. As can be seen in Table 5, these algorithms each have their own unique test sequences. In order to have an understanding of how it is implemented, we will use MARCH Y as an example. Depending on the method that is being utilized, each march sequence could need a different amount of clock cycles to complete. At instance, in MARCH Y, the first sequence (w0) takes one clock cycle for each memory address, but the second sequence (r0, w1, r1) takes three clocks for each memory location, and so on. Figure 8 depicts the state sequence for the algorithm known as the March Y Algorithm.

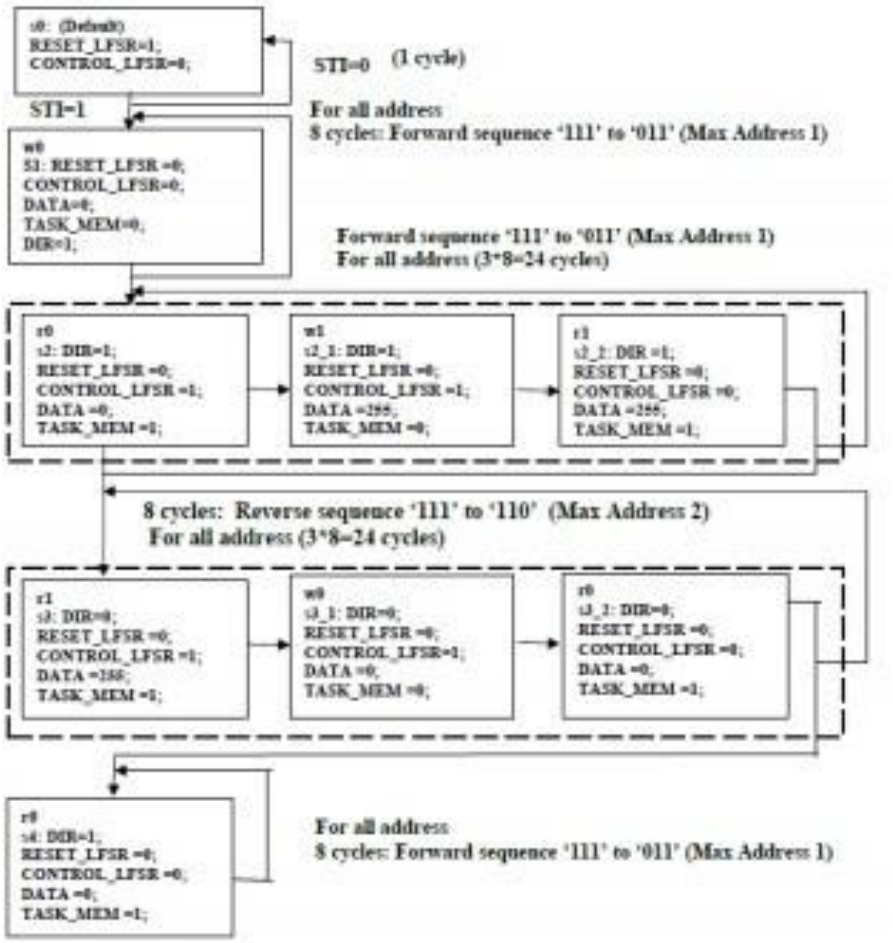


Figure 3.11 State sequence for March Y Algorithm

The first sequence, "(w0)," indicates that the value "0" will be written to all of the addresses (as created by LFSR) in any address sequence. This implies that the sequence may be carried out in either an ascending or descending order of sequence. Because accessing each memory location requires one clock cycle, a total of eight cycles are necessary to access all eight locations. The second sequence, which is represented as (r0,w1,r1), indicates that the series advances in an ascending order of address. In the first cycle, the value '0' is taken from an address, then in the second cycle, the value '1' is written to that address, and finally, in the following cycle, the value '1' is taken from that address once again (i.e. the whole sequence is executed on the same address and then next address in the increasing order is generated, so it takes 24 cycles for all 8 locations). After the second sequence has been carried out for each address, the third sequence, which is denoted by the notation "r1,w0,r0," is carried out in the same fashion but in the

reverse order of the addresses (i.e. the whole sequence is executed on the same address and then next address in the decreasing order is generated, so it takes 24 cycles for all 8 locations). The last sequence, r0, is carried out last and does not have any requirements on the order in which the preceding sequences are carried out. This means that it may be carried out in either an ascending or descending order of sequence, resulting in a total of 8 cycles for each of the 8 locations.

CHAPTER 4

EXISTING METHOD

INTRODUCTION

One of the many methods available for testing combinational circuits is known as the BIST method. Other methods also exist. BIST stands for "break-in-sequence testing," and refers to a system or process that enables a machine or circuit to test itself [1]. The fundamental concept behind BIST is to add test circuitry together with the regular system circuitry in order to validate that the system is operating as it should [1]. As can be seen in Figure 4.1, the Test Pattern Generator (TPG), the Circuit Under Test (CUT), and the Output Response Analyzer (ORA) are all components of the overarching architecture that constitutes BIST. The TPG is responsible for the generation of patterns that are then fed into the CUT. The CUT then carries out its purpose and provides the outputs for each test pattern. The outputs are then examined by the ORA, which does so by comparing the obtained output with the predicted outputs that have been saved in ROM. Following this comparison, a pass/fail signal is created, which shows whether or not the circuit has any errors. The difficulty of testing chips likewise grows in proportion to the amount of transistors that are included inside a chip. Consequently, it is impractical to save the predicted output or the real value of a CUT. The testing of a combinational circuit is discussed in this work, and it incorporates both a power-efficient TPG and an ORA that has been improved. The single stuck-at fault model is used here for the sake of testing. Due to the fact that it has been shown via a variety of studies that high single fault coverage for any problem translates to high multiple fault coverage, the suggested technique may be expanded for the purpose of discovering numerous faults that are trapped at the same location [1].

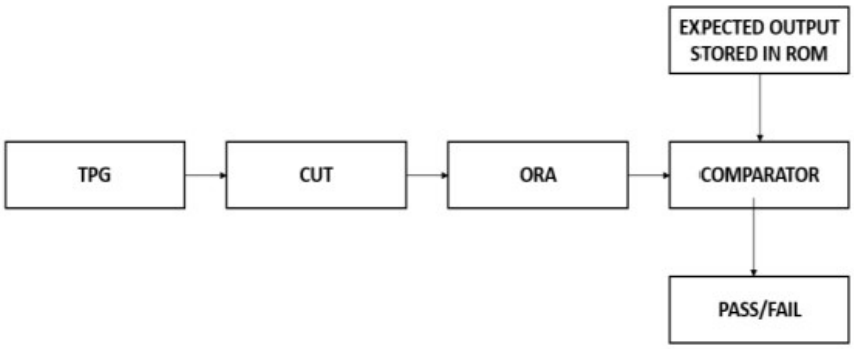


Figure 4.1. General architecture of BIST

TEST PATTERN GENERATOR

Producing test patterns for the CUT is the responsibility of a BIST component known as a Test Pattern Generator. These test patterns are fed into the CUT, and the outputs that correspond to each test pattern are received once the test patterns are processed. Conventional LFSR The traditional LFSR is the TPG that is used most often in BIST [1]. A standard N-bit LFSR has the ability to make 2N-1 patterns. Because it generates these patterns in an unpredictable manner, this kind of TPG is referred to as pseudo-random TPG. This TPG is unable to construct the pattern with full zeros. Figure 2 depicts a standard 4-bit LFSR (external) with a polynomial that reads as follows: x4+x+1. Because standard LFSR generates patterns with a large number of transitions, these patterns also produce patterns with a high level of power. Bit-swapping is a method that has been devised and included into the traditional LFSR in order to minimize the number of transitions that are required.

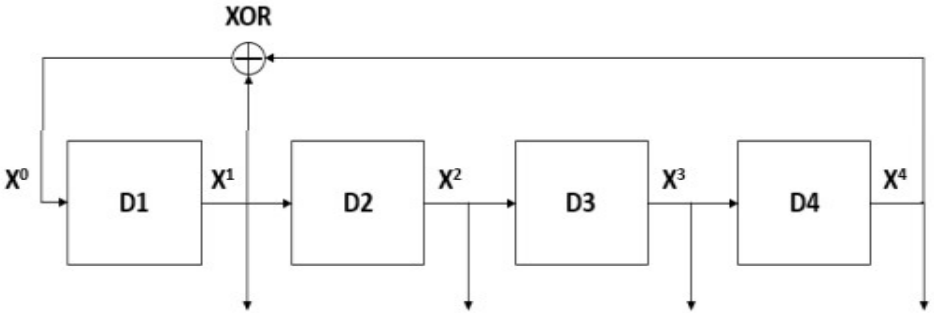


Figure 4.2. 4-bit conventional LFSR

4.3 BIT-SWAPPED LFSR

Bit swapping is a method that is used to minimize the switching activity, also known as the number of transitions; this, in turn, helps lower the amount of power used. By combining a standard LFSR with additional 2x1 multiplexers, it is possible to create an LFSR that is capable of bit-swapping [6]. The design of an n-bit bit-swapped LFSR may be seen in Figure 4.3. The multiplexers are added to the traditional LFSR in order to reorder the patterns in such a manner that the switching activity is minimized. This is accomplished by reducing the number of patterns that need to be switched. It is possible to cut the total number of transitions by as much as 25 percent [7].

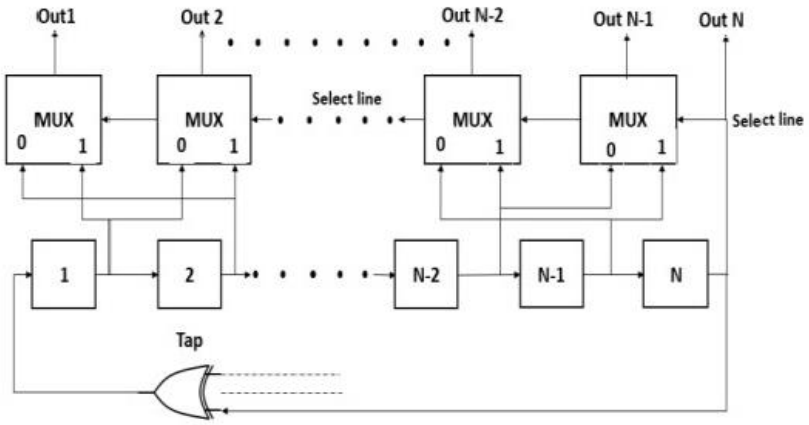


Figure.4.3. General architecture of BS-LFSR

4.4. OUTPUT RESPONSE ANALYZER

Analyzing the outputs that were collected from the CUT is the responsibility of a component of BIST known as an Output Response Analyzer. When it comes to interpreting the results produced by CUT, the approach known as signature analysis is by far the most used [1].

Traditional MISR is a kind of MISR that is used for signature analysis. The purpose of this MISR is to perform the operation of dividing the output polynomial of the CUT by the MISR's own polynomial. The remaining portion is referred to as the golden

reference or the golden signature. The design of a standard MISR is seen in figure 4. There will be a variety of distinct output polynomials when numerous output CUTs are considered. Because of this, performing an analytical trace of the operation of this MISR in order to validate the golden signature will be challenging [8]. This traditional technique will also be unable to implement if the number of outputs produced by the CUT is more than the number of inputs that it receives..

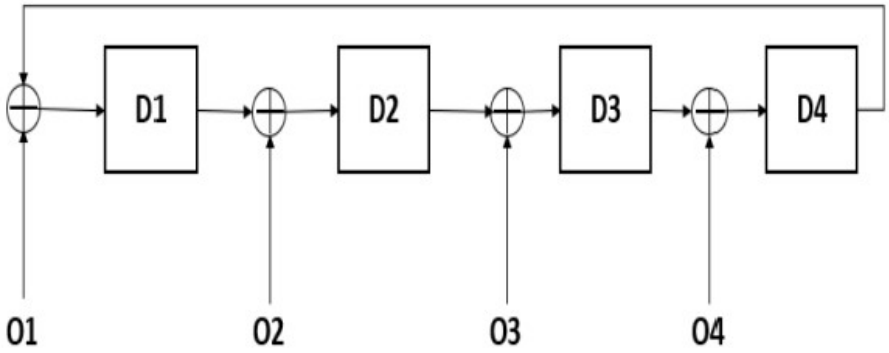


Figure.4.4. 4-bit Conventional MISR

4.5 MODIFIED MISR

A single (resultant) polynomial is obtained by the process of aggregating all of the outputs of CUT in this MISR's modification procedure. This polynomial is then sent to a Single Input Signature Register (SISR). All of the output polynomials are XORed at one point in the updated MISR, which can be seen in Figure 4.5. (aggregated). Analytical retracing of the action of the MISR algorithm is feasible due to the fact that the resulting is a single polynomial. This enhanced MISR has the potential to be the superior choice for CUTs in which the number of outputs is higher than the number of inputs. The limitations that are inherent to the traditional MISR are circumvented by this MISR.

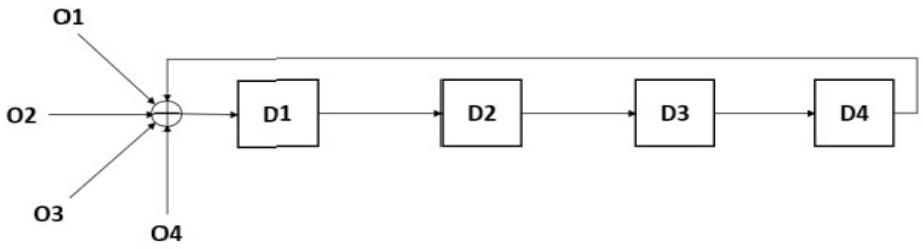


Figure4.5: 4-bit Modified MISR

4.6. EXISTING WORK

In this work, a power-efficient BIST design is given for implementation. The suggested BIST's internal structure is seen in figure 4.6. The BS-LFSR algorithm is employed as the TPG in this BIST, while the Modified MISR algorithm is used as the ORA. This BIST is more power efficient than others because of the BS-LFSR, which is responsible for the power reduction of up to 25 percent.

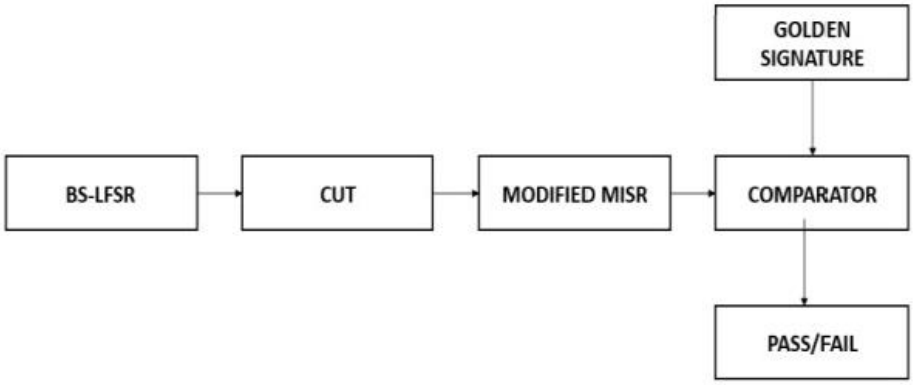


Figure.4.6. Architecture of proposed BIST

4.7 BS-LFSR as TPG

As can be seen in Figure 7, the BS-LFSR has its select line for the 2x1 multiplexer allocated to the fourth bit, which is signal d. The bit switching takes place when this signal d is a '0', which means that the first bit (signal a) and the second bit (signal b) are switched places. When this signal d reads "1," there is no exchange taking place. The swapping approach does not apply to signal d since it is the selection line, hence this eliminates the need for it. The BS-LFSR generates many outputs, including O1, O2, O3, and O4, which are then fed into the CUT.

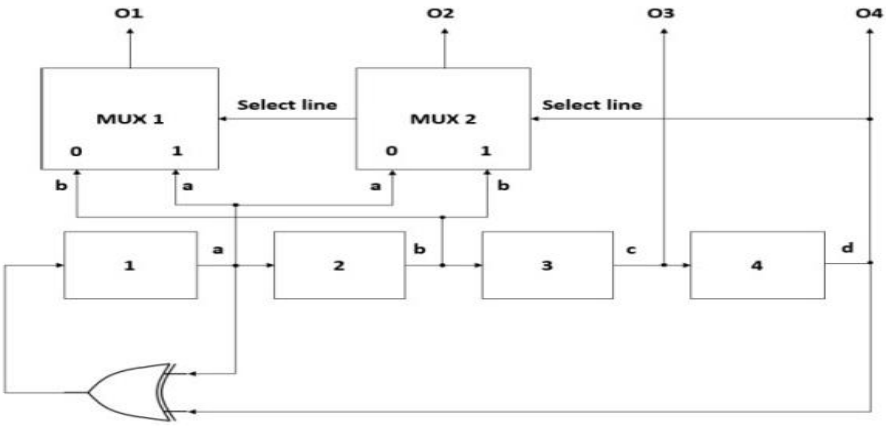


Fig. 4.7. 4-bit Bit swapped LFSR

Circuit Under Test (CUT) :The CUT that was used for the BIST is shown in Fig.8. The combinational circuit in question contains not one but two outputs, denoted O1 and O2. Utilizing the patterns produced by the 4-bit bit-swapped LFSR to create the truth table for the CUT, as illustrated in Table 4.1, is accomplished by using the value "1000" as the starting seed.

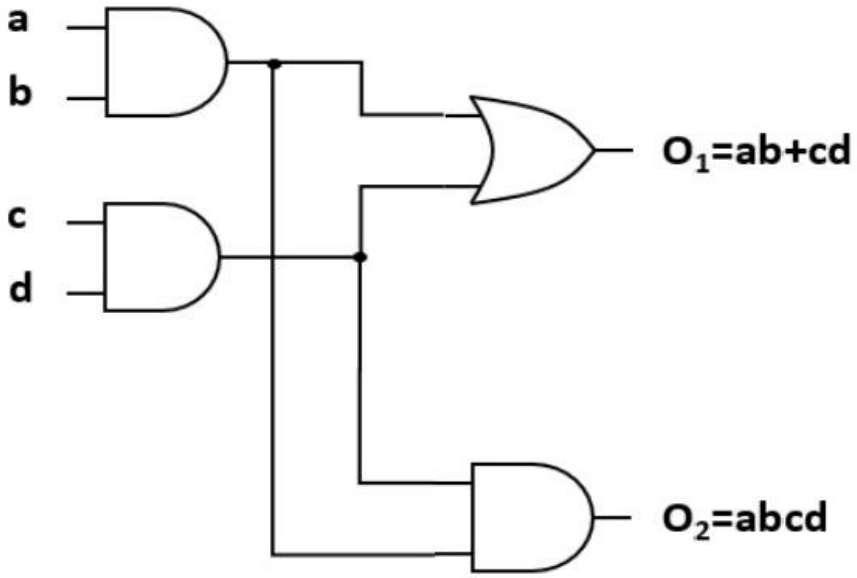


Figure. 4.8. Circuit Under Test

TABLE I. TRUTH TABLE OF CUT

a	*b*	*c*	*d*	*O1*	*O2*	*Polynomial*
1	0	0	0	0	0	x^{14}
0	1	0	0	0	0	x^{13}
0	0	0	1	0	0	x^{12}
0	0	1	0	0	0	x^{11}
1	1	0	0	1	0	x^{10}
0	1	0	1	0	0	X^{9}
0	0	1	1	1	0	X^{8}
1	1	0	1	1	0	X^{7}
1	0	1	0	0	0	X^{6}
0	1	1	0	0	0	X^{5}
1	1	1	0	1	0	X^{4}
0	1	1	1	1	0	X^{3}
1	1	1	1	1	1	X^{2}
1	0	1	1	1	0	X^{1}
1	0	0	1	0	0	X^{0}

Output polynomial of O1= $x^{10} + x^{8} + x^{7} + x^{4} + x^{3} + x^{2} + x^{1}$
Output polynomial of O2= x^{2}

Table 4.1.Truth table of CUT

Modified MISR as ORA

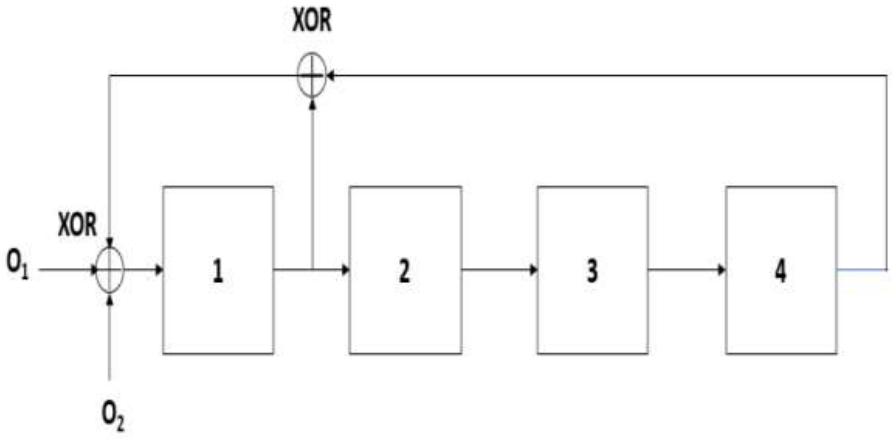


Figure.4. 9. 4-bit Modified MISR

$$
\begin{array}{r|l}
 & x^6 + x^4 + x^2 + x^1 \\
\hline
x^4 + x + 1 & x^{10} + x^8 + x^7 + x^4 + x^3 + x^1 \\
 & x^{10} + x^7 + x^6 \\
\hline
 & x^8 + x^6 + x^4 + x^3 + x^1 \\
 & x^8 + x^5 + x^4 \\
\hline
 & x^6 + x^5 + x^3 + x^1 \\
 & x^6 + x^3 + x^2 \\
\hline
 & x^5 + x^2 + x^1 \\
 & x^5 + x^2 + x^1 \\
\hline
 & 0 \\
\hline
\end{array}
$$

Figure.4.10. Operation of modified MISR

The suggested BIST has the capability of identifying individual faults in the circuit that are stuck-at. Because this suggested technique uses the stuck-at fault model, the circuit has a number of single stuck-at faults. The reason for this is given in the previous sentence. In this concept, either an input signal or an output signal is fixed at the value 0 or 1, respectively. The use of a power-efficient TPG (BS-LFSR) and a modified MISR are integrated in the proposed BIST, which distinguishes it from the BIST that is

already in use. This is the main difference. However, despite the fact that the modified MISR already exists and is superior than the standard MISR [8, it is not used nearly as often as the conventional MISR is. Because of this, the BIST that was suggested is unique in comparison to traditional BIST. When compared to the technique provided in [3], this method is superior since it allows for a power savings of 25% inside the proposed BIST and enables the modified MISR to be utilized for monitoring the functioning of the BIST.

CHAPTER 5

PROPOSED METHOD

INTRODUCTION

Since the beginning of this decade, Very Large-Scale Integration (VLSI) has seen a significant increase in the integration density it can achieve. Because of this, the system-on-chip was realized [1]. When testing VLSI chips with external hardware, the process may be exceedingly challenging. It is highly challenging to test such VLSI circuits because of the large amount of test data that is needed. The traditional testing technique involves storing a significant quantity of test data outside in order to test the Circuit Under Test (CUT) [2]. The BIST is an alternate testing instrument that may be used outside. The development of test patterns and the analysis of responses are both carried out inside the chip itself in BIST. In addition to these advantages, using BIST may also raise the testing speed while simultaneously improving the testing quality [3]. VLSI, or very large scale integration, is a kind of cell technology that is based on semiconductors and is used to construct integrated circuits by merging thousands of transistors. Both the microprocessor and the microcontroller are examples of devices that are based on VLSI.

Integrated circuits may include a central processing unit, random access memory, read only memory (ROM), and other logic devices [4]. The VLSI technology integrates several kinds of devices into a single chip. The advancement of VLSI technology enables embedded systems to be created for specialized applications at prices that are within reach of all members of the society. The primary necessity of the VLSI design is to assess the dependability of the produced goods [5]. The approach of structured design is used for the purpose of making testing of VLSI circuits easier. A semiconductor design that cannot be tested may need more time to test and develop. One of the most important steps in the design and production of integrated circuits is sorting the chips on the wafer based on their quality. The quality of the goods and the degree of satisfaction experienced by customers are directly linked to early detection of defective integrated circuits (ICs) during manufacturing.

The methodologies Design for Testing (DFT) [6] and BIST are used to test the chip during the design stages to determine whether or not it is stuck-at-fault one hundred percent of the time. DFT is equipped with a number of different methodologies, including as the scan design method, on-chip hardware for the development of test patterns, and data compression methods, that may boost controllability and observability. The BIST scheme is formed by combining a number of different DFT approaches [7]. Combined test pattern creation, built-in evaluation, self-test, partitioning, multiplexer test point insertion, serial scan, and random test pattern are some of the key BIST techniques. At the design stage itself, there are a variety of methods available to identify any defects that may exist in the chip [8]. During the design stage of the chip itself, design verification processes and computer assisted design procedures are used in order to locate the error that has been introduced. The production test will be able to determine whether or not there is an error in the manufacturing process. It is not uncommon for the chip to develop physical faults, which, if left unchecked, will cause the chip to fail to perform the function for which it was designed [9].

Bulk silicon flaws, substrate mounting defects, substrate surface faults, bonding defects, particle contamination, thermal mismatch electrical stability, oxide defects, and metallization defects are the most common types of defects that occur [10]. The stuck at fault model provides an explanation of the underlying physical causes of the stuck at '0' and trapped at '1' faults. The stuck at fault model is adequate on its own to detect the various defects described in the previous paragraph. Test patterns are created by the use of the stuck at fault concept [11]. BIST stands for "back-instruction self-test," and it is a method of testing a circuit while it is being tested by including the testing operations directly into the CUT. The major contributions of this work are as follows:

- Implementation of an HML-BIST using LFSR modules with activity controlling.
- Design of LFSR based random number generators for write address, read address and write data, where activity factor is used to generate the non-repeated random numbers.
- Implementation of space comparator for identifying the errors presented in the data stored in memory.

5.2. PROPOSED SYSTEM

The proposed HML-BIST algorithm is based on the operation of checking the circuit under test. The important structures of the BIST architecture are test pattern generator, RAM output response analyzer and memory. The general BIST algorithm consists of nine steps.

Table 5.1. BIST Algorithm

Step 1: Identify the number of inputs(N) and outputs of Circuit under test.
Step 2: Generate 2N number of test pattern.
Step 3: Store the actual output in ROM for each test pattern.
Step 4: Apply the test pattern 1 and observe the output in the output response analyzer.
Step 5: The comparator compares the output signature with the golden signature.
Step 6: If there is no fault go to step 4 and test for the next test pattern.
Step 7: Check for the end of the test pattern.
Step 8: If there is no fault for all the test pattern declare the circuit under test is good.
Step 9: Declare the CUT is good or fault

The HML-BISTapproach that has been suggested using LFSR-based activity factor regulating may be shown in Figure 5.1. The test pattern generator, which makes use of LFSR, the space comparator-based output analyser, and the random access memory are the three essential components of the BIST (RAM). The generation of the necessary test pattern for the circuit that is now being evaluated is the job of the test pattern generator. In the realm of test pattern 3 generators, some examples are the LFSR, the counter, and RAM that already has testing data stored in it. The Response Analyzer is a sort of Comparator that retains model outputs for the purpose of comparing them with the actual outputs of the circuit that is being tested. A circuit known as the test controller is responsible for sending command signals to the test pattern generator in order to make test patterns available for testing. In addition to this, it sends signals to the space comparator, which causes it to compare the current output to the output that has previously been stored.

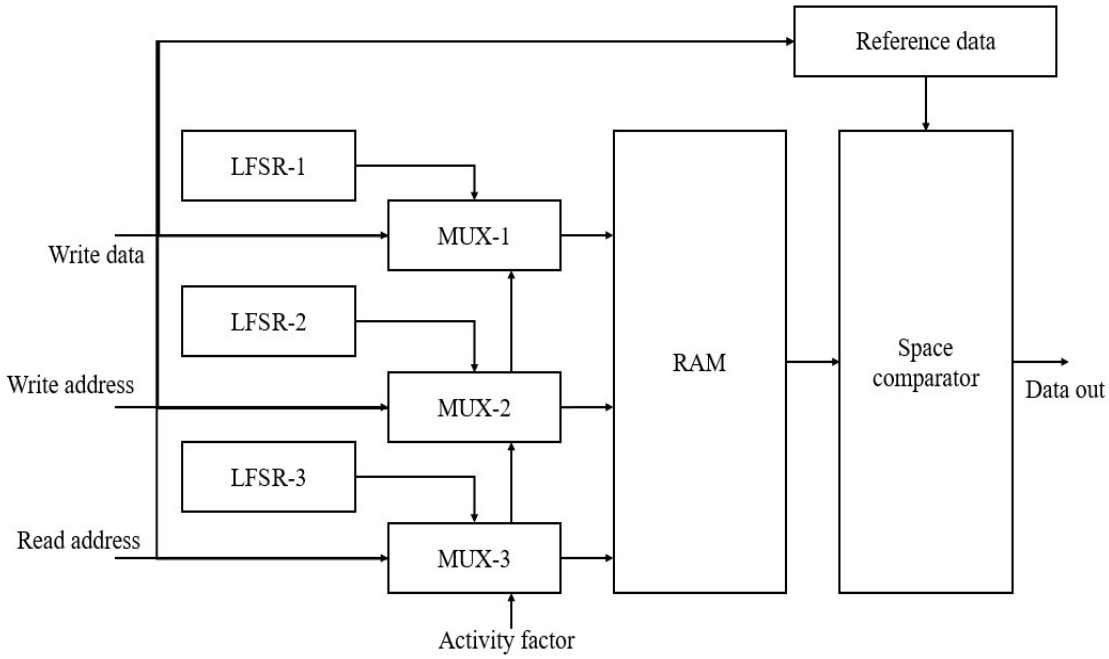


Figure 5.1. Proposed HML-BIST architecture.

The RAM is where all of the functions relating to the test are carried out. The fault model is developed via the process of coding. By writing code in Xilinx software, it is possible to generate a stuck at 1 fault as well as a stuck at zero error. The output of the output space comparator provides information that may be used to diagnose the problem. For a fault that is stuck at 1, all of the output may be high, whereas for a fault that is trapped at 0, all of the output could be low. Therefore, the output space comparator may be used in order to investigate the nature of the issue. The BIST incorporates both the circuit that generates the test pattern and the circuit that is being tested. When producing the test vector for the circuit that is being tested, LFSR is an essential component to have. In the LFSR-based test pattern generation that is being suggested, a total of 12 outputs are produced. The 12 outputs of the LFSR are converted by the isolation circuit into four inputs that are then used by the s27 sequential logical circuit.

The circuit being tested accepts as inputs the four outputs that are produced by the isolation circuit, processes those inputs, and then produces just one output. The output response analyzer is responsible for doing analysis on the CUT's outputs. In order to determine whether or not the circuit is functioning properly, the output response analyzer

compares the output of the CUT with memory. The circuit that is being tested will, during its usual mode of operation, receive signals from the input sources and create output signals that are sent to other devices. It will not accept any signals that are connected to BIST. Only the CUT will be the component that gets signals from the test pattern generator while the BIST is operating. The response analyzer will be used to examine how the CUT responds to various stimuli. The signals received from the response analyzer are compared with the reference signals that have previously been saved in the chip. The comparator is responsible for producing error signals. The error signals reveal whether or not the circuit being tested is functioning properly.

The approach known as BIST is included into the embedded system. When creating the embedded system for the BIST approach, there are four characteristics that need to be taken into consideration. These include hardware overhead, test set size, fault coverage, and performance overhead. If there are any mistakes at all in the test pattern that is generated by the test pattern generator, the space comparator will not provide an error signal and will instead show that the CUT is error free. Aliasing or masking are two names that are sometimes used to refer to this unwanted phenomenon. The term "test set size" refers to the total number of test patterns that are generated by the test pattern generator. If the size of the test set is increased, then the fault coverage will increase as well. If the size of the test set is too low, then it will not be able to cover all of the errors. The term "hardware overhead" refers to the supplementary hardware that must be installed in order to implement BIST. When implementing BIST in an embedded system, having additional hardware is not something that is ideal. In the BIST technique, it is preferable to use a smaller number of pieces of hardware for a larger circuit that is being tested. The use of BIST approach has the potential to sometimes interfere with the typical operation of the circuit that is being tested. During the usual functioning of the CUT, there is the possibility of a delay in responding. The term "performance overhead" refers to this unwanted quality. Because of this, there is a possibility that the consequences will be more severe than the hardware overhead. For a more successful application of the BIST technique in embedded systems, the aforementioned four characteristics need to be taken into consideration.

5.3 LFSR

When it comes to testing VLSI circuits, there are a plethora of test pattern options at your disposal. The researchers are generating a large number of new control methods each day and contributing a significant amount of labor to the study. Pseudo-random pattern is formed by a string of ones and zeros that are entered in a haphazard manner. This pattern is utilized as a testing vector for digital circuits. Pseudo-random pattern generator is the primary use for the Low Frequency Shaping Register (LFSR). This method creates a greater variety of patterns than the ATPG bus while still producing fewer patterns than pseudo pattern generation. When compared to other methods, the production of pseudo-random patterns often requires a longer amount of time. Additionally, in comparison to previous strategies, this method calls for a smaller amount of hardware, a lower performance overhead, and a reduced amount of design work.

In order to produce the pseudo-random pattern, the LFSR is put to use. The length of the string, also known as the seed, is either comparable to or less than the length of the LFSR. In terms of LFSR, the seed and test vectors may be obtained by solving a linear set of algebraic equations. Figure 2 depicts a general example of the LFSR's architectural make-up.

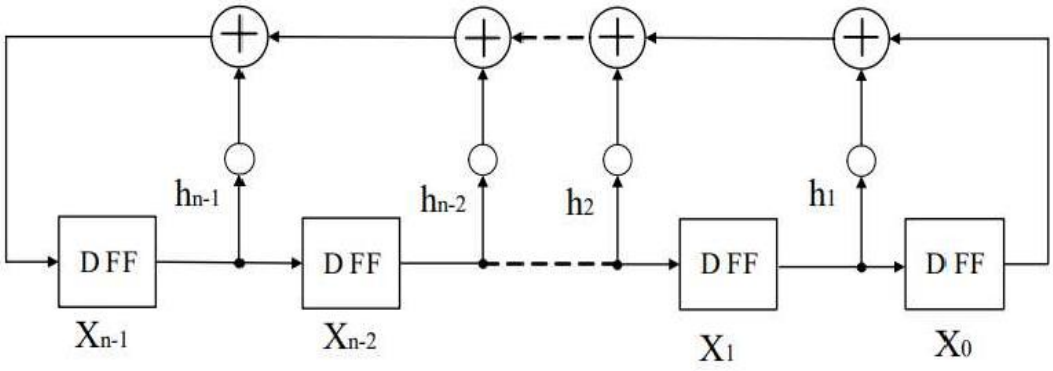


Figure 5.2. A standard LFSR structure.

The test pattern is generated by a significant number of D flip flops, which make up the majority of the LFSR. In order to provide feedback and achieve pseudo random pattern creation, the outputs of D flip flops are mixed with the outputs of other D flip

flops in a certain sequence. The LFSR may be realized by the use of the actual digital circuit. Figure 5.4 depicts the n stage LFSR in its entirety.

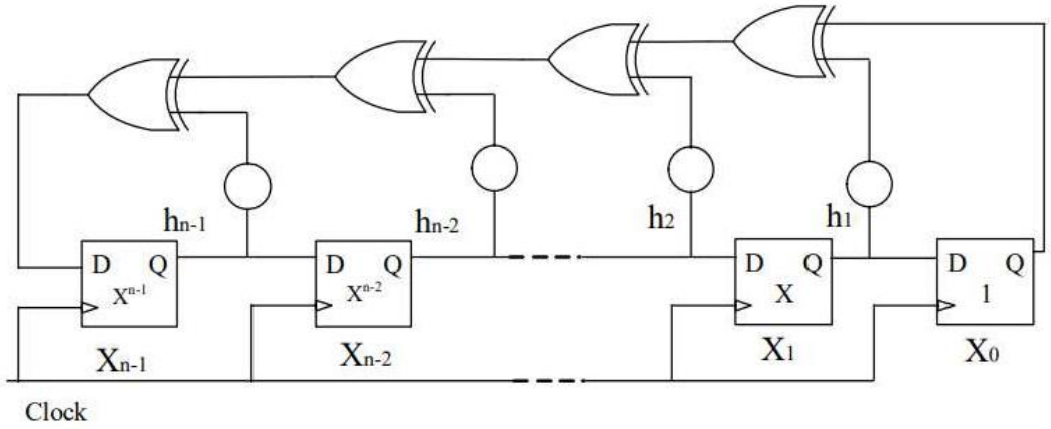


Figure 5.3.n-stage LFSR with actual digital circuit

The construction of an n-stage LFSR that is capable of producing n output lines using the outputs of a D flip-flop. In addition, the output of one D flip flop is mixed with the output of another D flip flop using an XOR gate, and the result is fed back into the first D flip flop. The clock pulse for all of the D flip flops originates from the same location. It is possible to produce the necessary Pseudo pattern from the LFSR using the appropriate connections for the EXOR gate.

CHAPTER-6

Xilinx ISE

Step 1: Select "NEW PROJECT" by clicking on it.

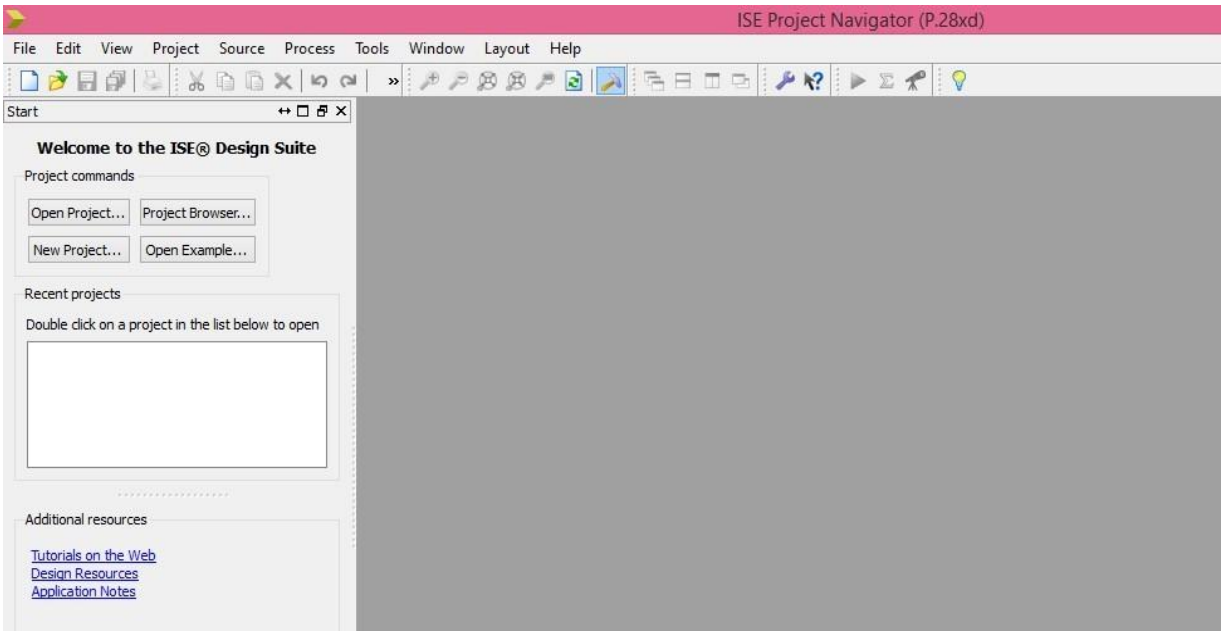


Figure 6.1. Select "NEW PROJECT" by clicking on it.

The second step is to choose a location and give the project a name (WRITABLE)

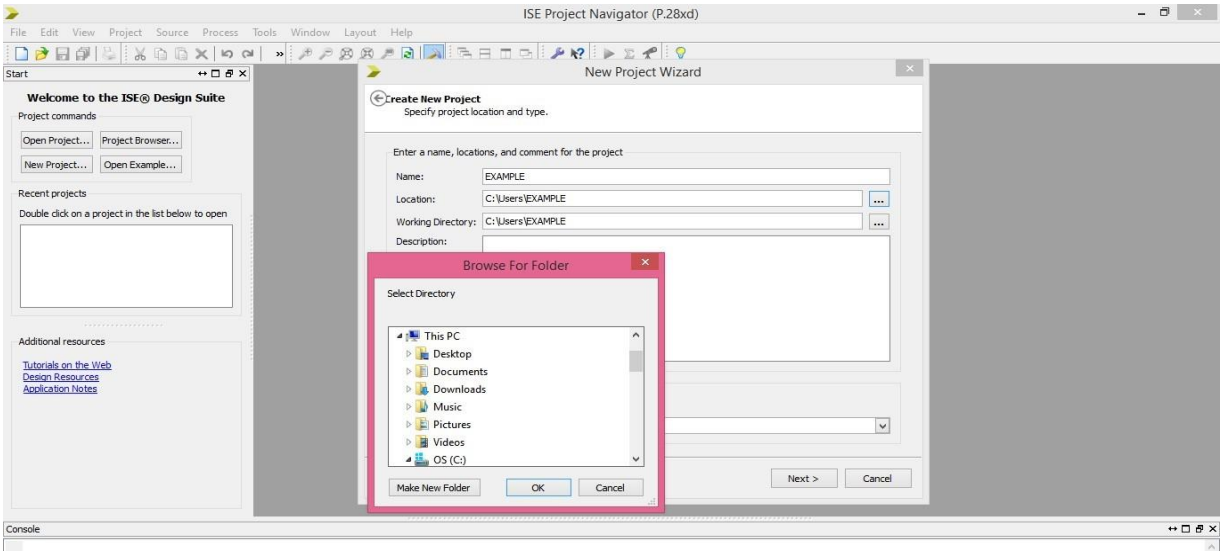
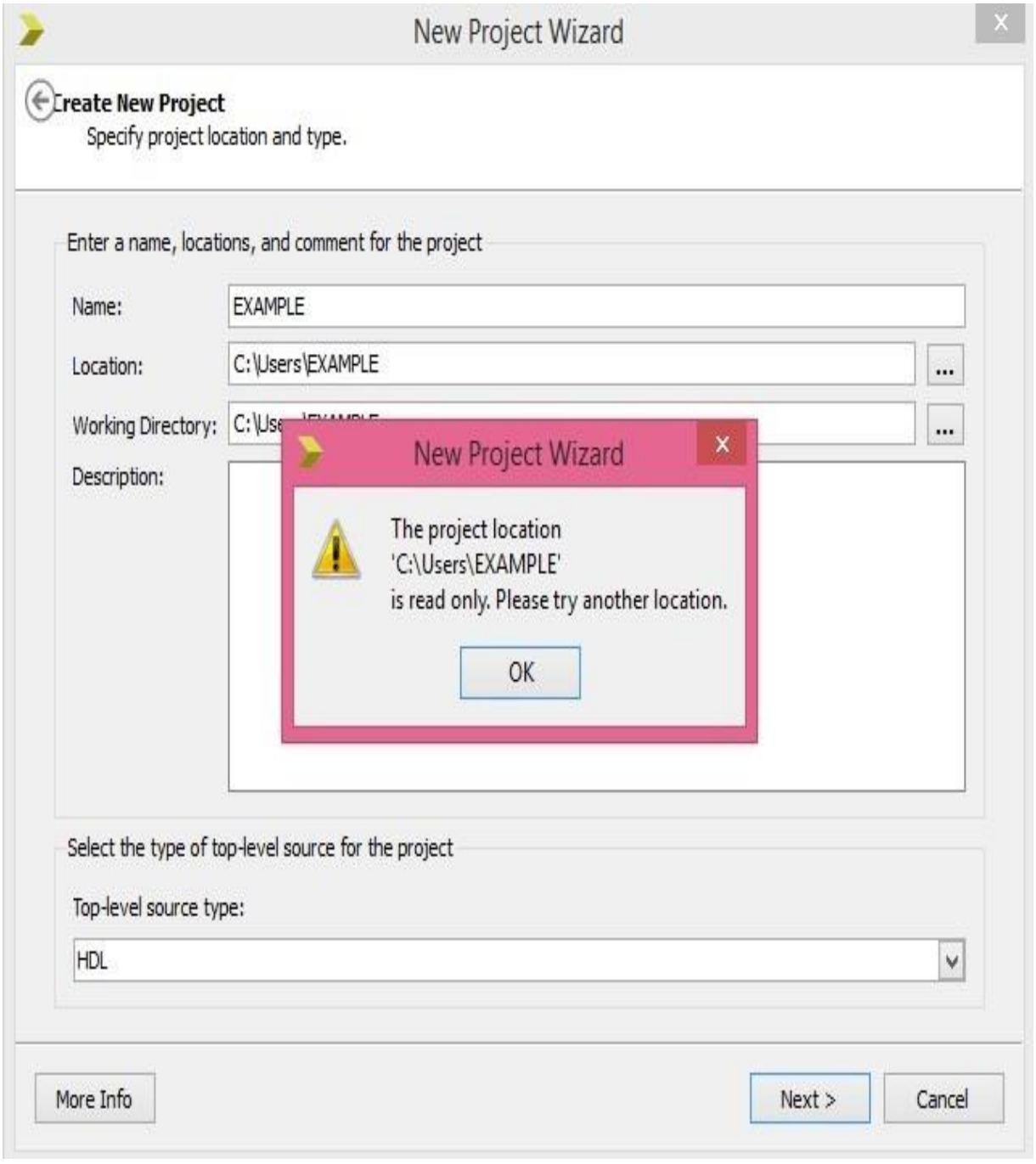


Figure 6.2. The second step is to choose a location and give the project a name

(WRITABLE)


New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name:
EXAMPLE
Location:
C:\Users\EXAMPLE
Working Directory:
Description:
New Project Wizard
The project location
'C:\Users\EXAMPLE'
is read only. Please try another location.
OK
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next >
Cancel

Step 3: DOUBLE-CLICK THE NEXT AND NEXT BUTTONS

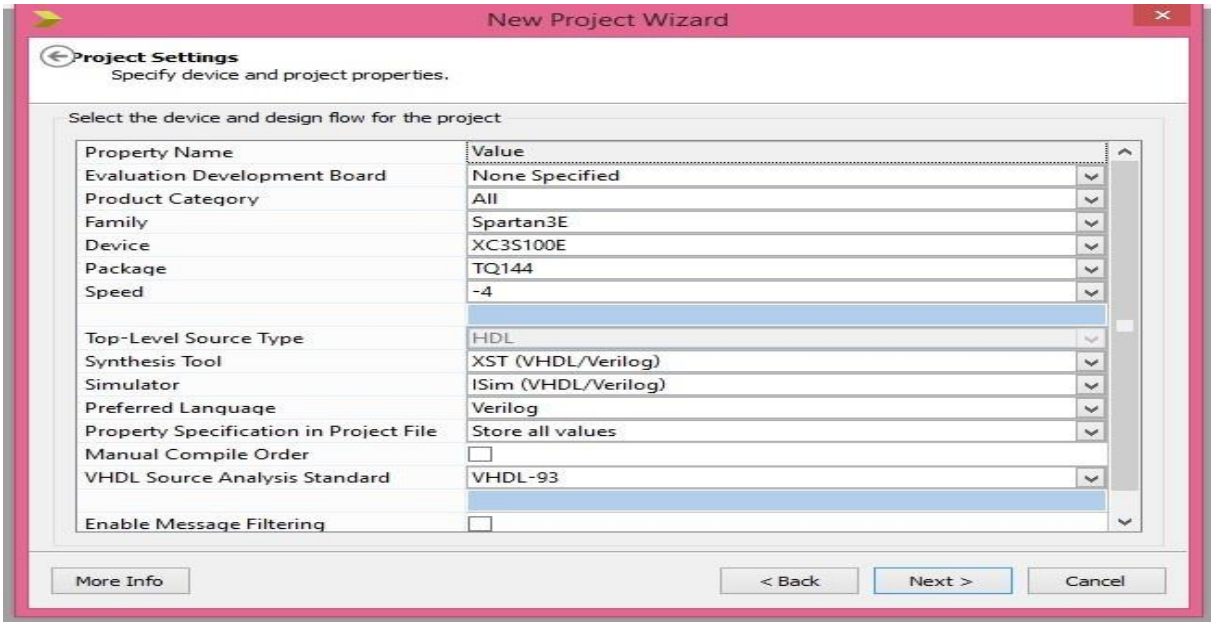


Figure 6.3 DOUBLE-CLICK THE NEXT AND NEXT BUTTONS

Step 4: CLICK ON FINISH

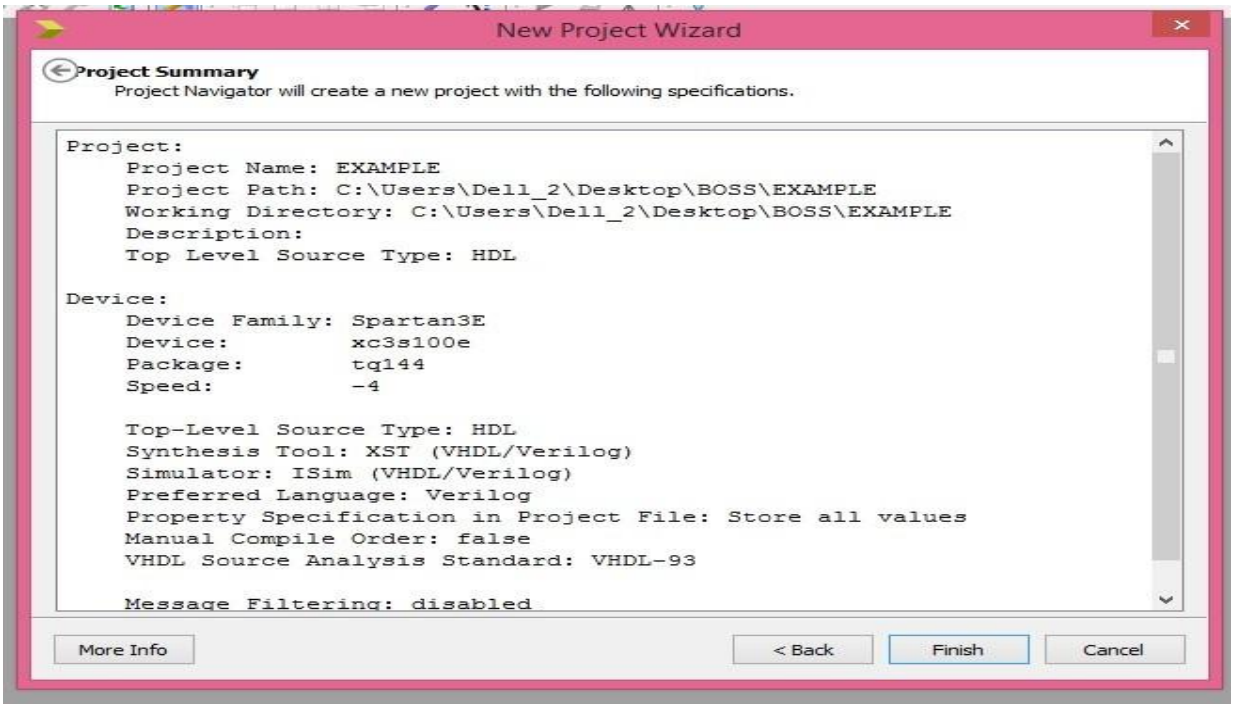


Figure 6.4 CLICK ON FINISH

Step 5: To add a source, first click on CHIP (XC...), then mouse-right-click, and last click on ADD SOURCE.

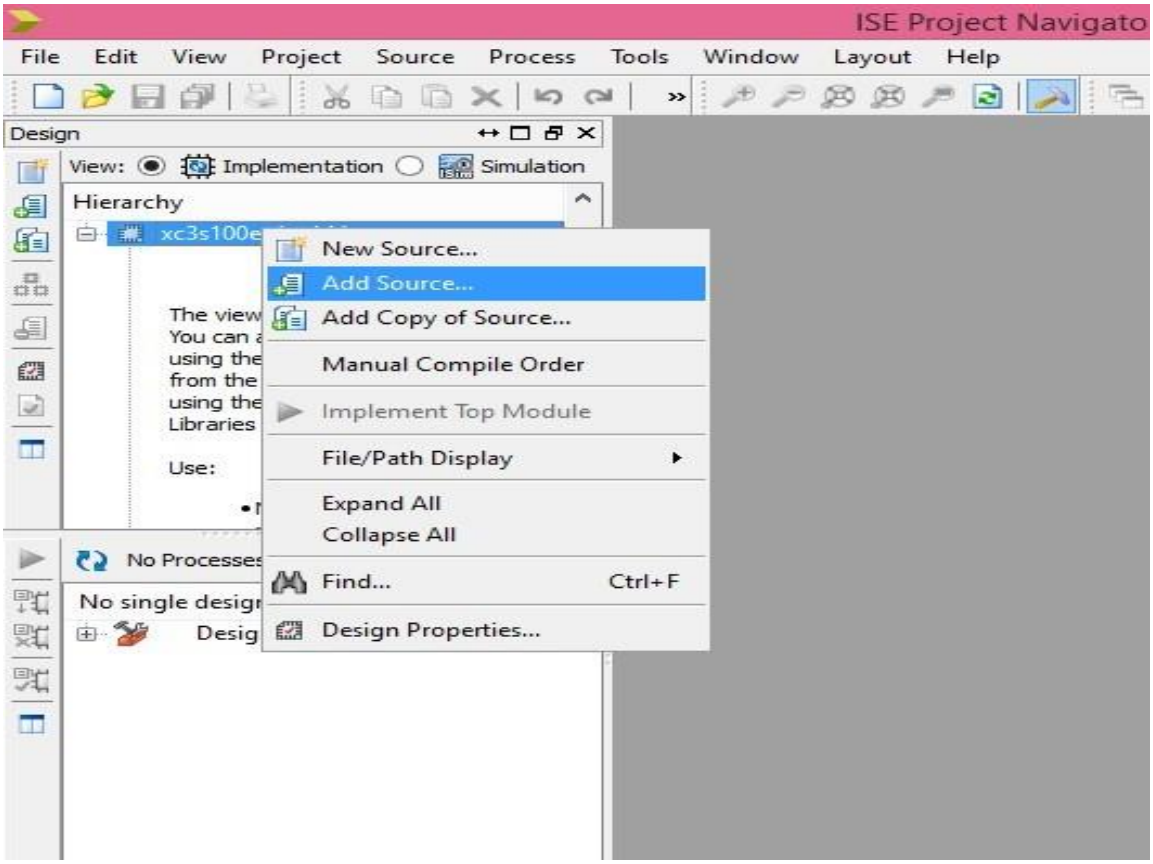


Figure 6.5 To add a source, first click on CHIP (XC...), then mouse-right-click, and last click on ADD SOURCE.

Step 6: SELECT THE LOCATION OF THE CODE THAT WAS PROVIDED BY THE DEVELOPER, ADD CODE (NOTE THAT ALL FILES MUST BE ADDED), AND CLICK THE OPEN BUTTON.

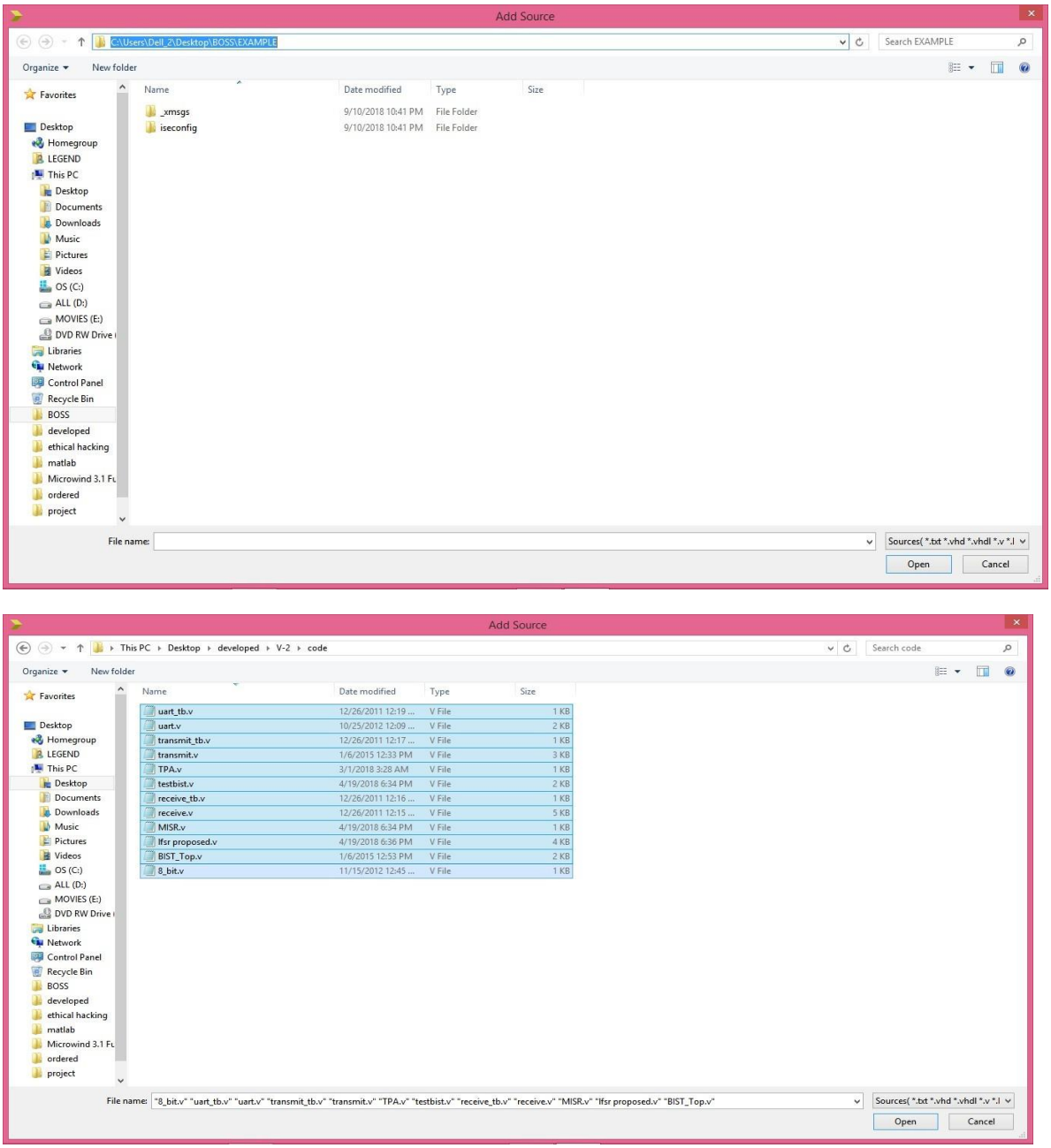


Figure 6.6select the location of the code that was provided by the developer, add code (note that all files must be added), and click the open button.

Step 7: CHOOSE THE SIMULATION, then choose the files you want to RUN.

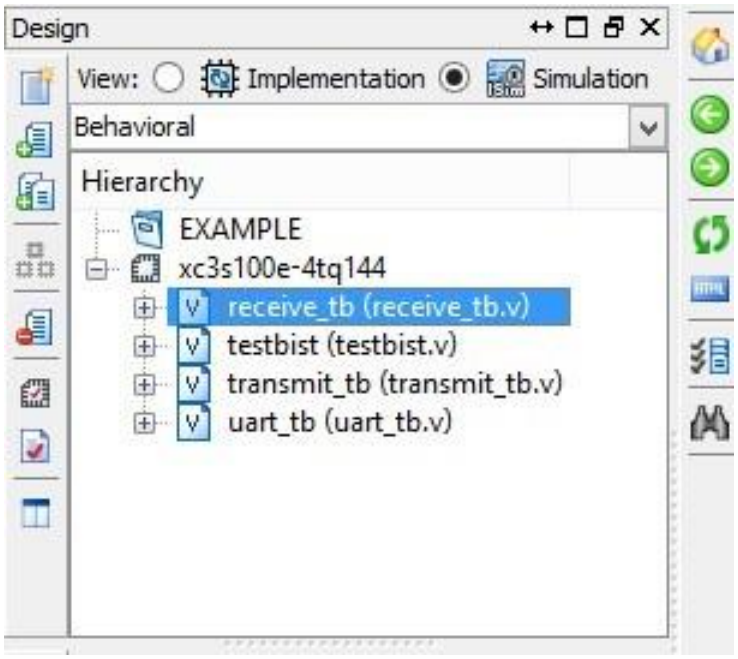


Figure 6.7 CHOOSE THE SIMULATION, then choose the files you want to RUN.

Step 8: simulate behavioral model after selecting the isim simulator. The isim window will open, if there are no mistakes.

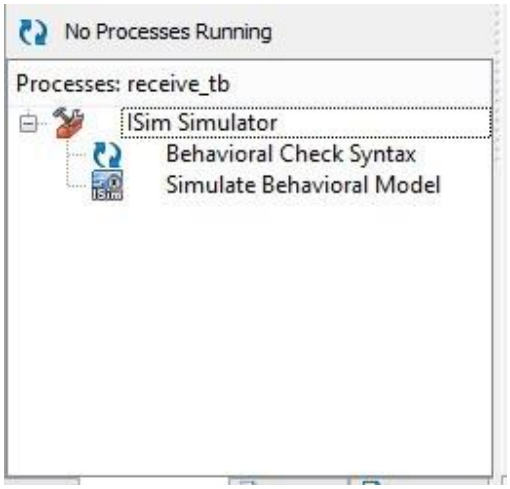


Figure 6.8 simulate behavioral model after selecting the isim simulator. The isim window will open, if there are no mistakes.

Step 9: ISIM WINDOW

select zoom to full view

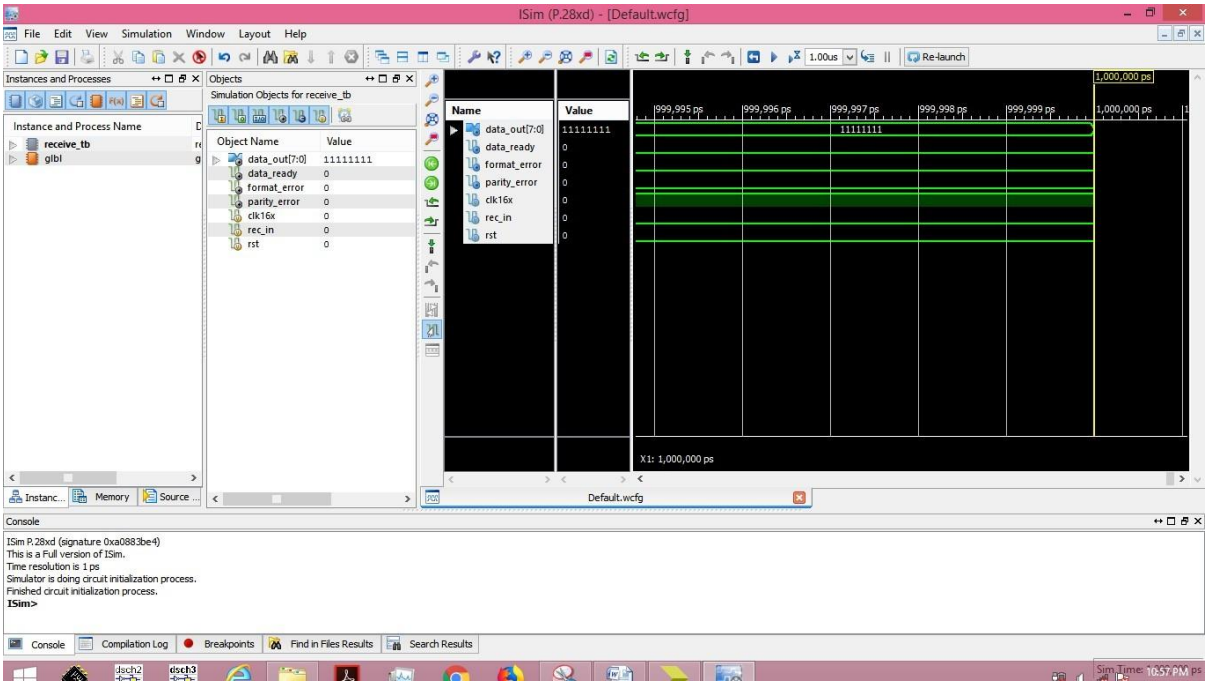


Figure 6.9 ISIM WINDOW

CHAPTER-7

SIMULATION RESULTS

EXISTING RESULTS

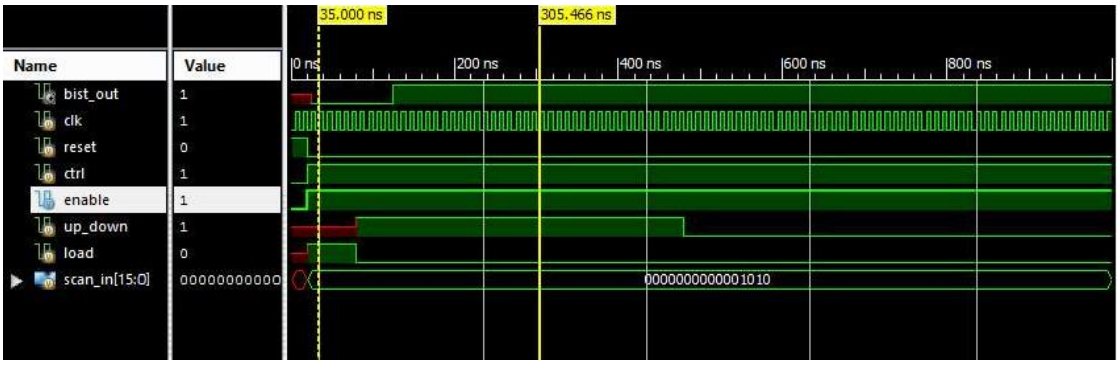


Figure 7.1 Simulation

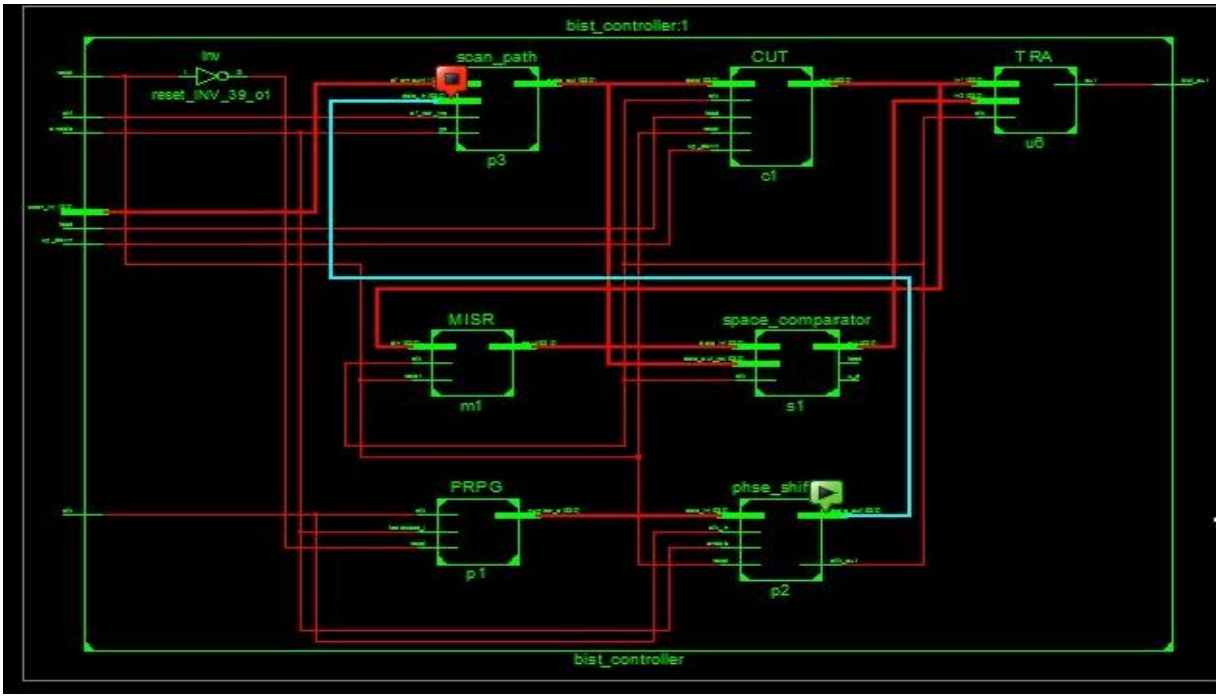


Figure 7.2 Rtl schematic

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	768	35200	2%
Number of Slice LUTs	6285	17600	35%
Number of fully used LUT-FF pairs	612	6441	9%
Number of bonded IOBs	23	100	23%
Number of BUFG/BUFGCTRLs	2	32	6%

Figure 7.3 Design summary

```
Data Path: u6/out to bist_out
                                   Gate     Net
  Cell:in->out      fanout         Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD:C->Q               2         0.232    0.283  u6/out (u6/out)
   OBUF:I->O                       0.000           bist_out_OBUF (bist_out)
  ----------------------------------------
  Total                            0.515ns (0.232ns logic, 0.283ns route)
                                           (45.0% logic, 55.0% route)
```

Figure 7.4 Time summary

Device	
Family	Virtex6
Part	xc6vlx75tl
Package	ff484
Temp Grade	Commercial
Process	Typical
Speed Grade	-1L

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	46	46560	0
Signals	0.000	122	--	--
IOs	0.000	52	240	22
Leakage	1.065			
Total	1.065			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.7	82.1	52.9

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	0.900	0.435	0.000	0.435
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Supply Power (W)	Total	Dynamic	Quiescent
	1.065	0.000	1.065

Figure 7.5 Power summary

PROPOSED RESULTS

Xilinx ISE software was used to create all of the BIST designs. This software programmed gives two types of outputs: simulation and synthesis. The simulation results provide a thorough examination of the BIST architecture in terms of input and output byte level combinations. Decoding procedure approximated simply by applying numerous combinations of inputs and monitoring various outputs through simulated study of encoding correctness. The use of area in relation to the transistor count will be accomplished as a result of the synthesis findings. In addition, a time summary will be obtained with regard to various path delays, and a power summary will be prepared utilizing the static and dynamic power consumption.

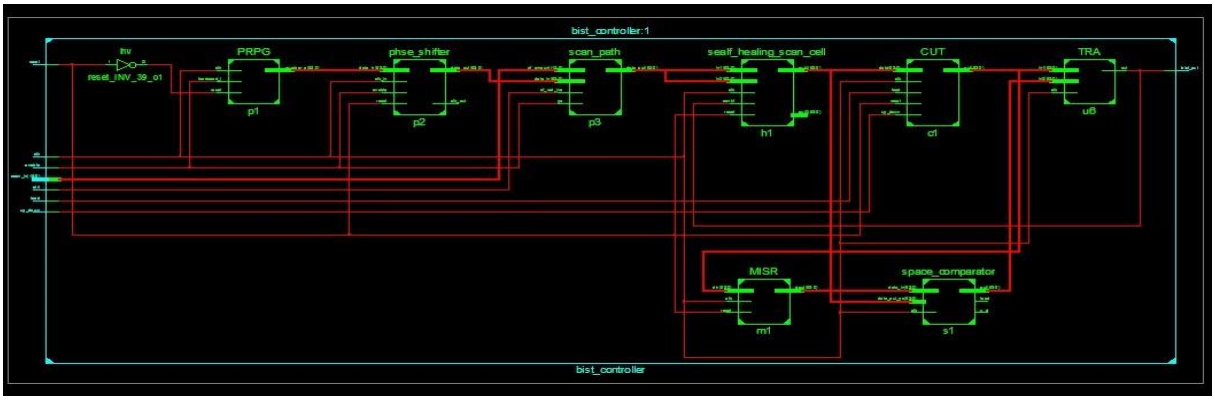


Figure 7.6 proposed schematic

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	512	35200	1%
Number of Slice LUTs	12142	17600	68%
Number of fully used LUT-FF pairs	348	12306	2%
Number of bonded IOBs	24	100	24%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	1	80	1%

Figure 7.7. Design summary.

Figure 7.7 shows the design (area) summary of proposed method. Here, the proposed method utilizes the low area in terms of slice LUTs i.e., 12142 out of available 17600. Further, the proposed method utilizes the slice registers as 512, out of available 35200.

Further, the proposed method utilizes fully used LUT-FF as 348, out of available 12306. Further, the proposed method utilizes buffers (BUF) as 2, out of available 32.

```
Data Path: u6/out to bist_out
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD:C->Q               1   0.232   0.279  u6/out (u6/out)
   OBUF:I->O                 0.000          bist_out_OBUF (bist_out)
  ----------------------------------------
  Total                      0.511ns (0.232ns logic, 0.279ns route)
                                     (45.4% logic, 54.6% route)
```

Figure 7.8. Time summary

Figure 7.8 shows the time summary of proposed method. Here, the proposed method consumed total 0.511ns of time delay, where 0.232ns of delay is logical and 0.279ns of delay is route.

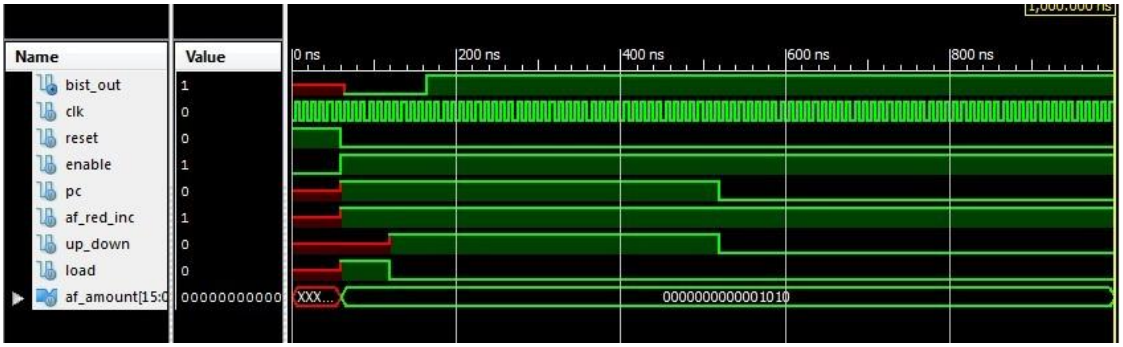
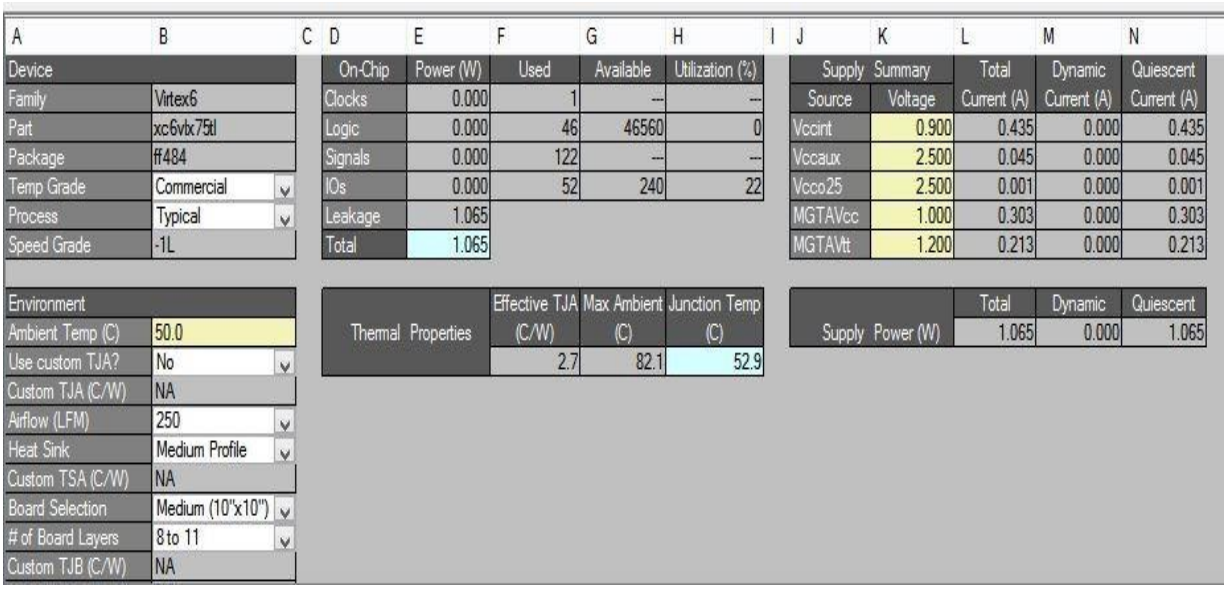


Figure 7.9. Simulation outcome.

Figure 7.9 presents the simulation outcome of proposed system. Here, clock (clk), reset, enable, program_counter(pc), activity_factor_reduction_increment (af_red_inc), up_down, load, and af_amount are the input data pins. Further, bist_out is the output pin. During the active high reset, system is intilized to zero and during active low reset, system starts work. The system is disable during the active low enable, pc, and system

starts work during active high enable, pc. If the load is active high, then the af_amount is loaded in BIST environment. Further, active high of af_red_inc resulted in increment of activity factor and active low of af_red_inc resulted in decrement of activity factor. In addition, active high of up_down resulted in increment counting and active low of up_down resulted in decrement of counting. Finally, active low of bist_out shows BIST fail condition and active high of bist_out shows BIST pass condition.



Device	
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Temp Grade	Commercial
Process	Typical
Speed Grade	-1L

Environment	
Ambient Temp (C)	50.0
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Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
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Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Supply Power (W)	Total	Dynamic	Quiescent
	1.065	0.000	1.065

Figure 7.10. Power summary

Figure 7.10 shows the power consumption report of propsoed HML-BIST. Here, the propsoed HML-BIST consumed power as 1.065 watts. Table 1 compares the performance evaluation of various BIST controllers. Here, the propsoed HML-BIST resulted in superior (reduced) performance in terms of LUTs, slice registers, LUT-FFs, time-delay, and power consumption as compared to conventional approaches such as MBIST [22], PSRG-BIST [23], and FT-BIST[24]. Further, the graphical representation of performance comparison is presented in Figure 8.

Table7.1. Performance evaluation

Metric	MBIST [22]	PSRG-BIST [23]	FT-BIST [24]	Proposed HML-BIST
Slice Registers	784	734	673	512
LUTs	18367	17352	15327	12142
LUT-FFs	826	736	635	348
Time delay (ns)	0.927	0.836	0.726	0.511
Power consumption (w)	32.482	24.1939	16.937	1.1065

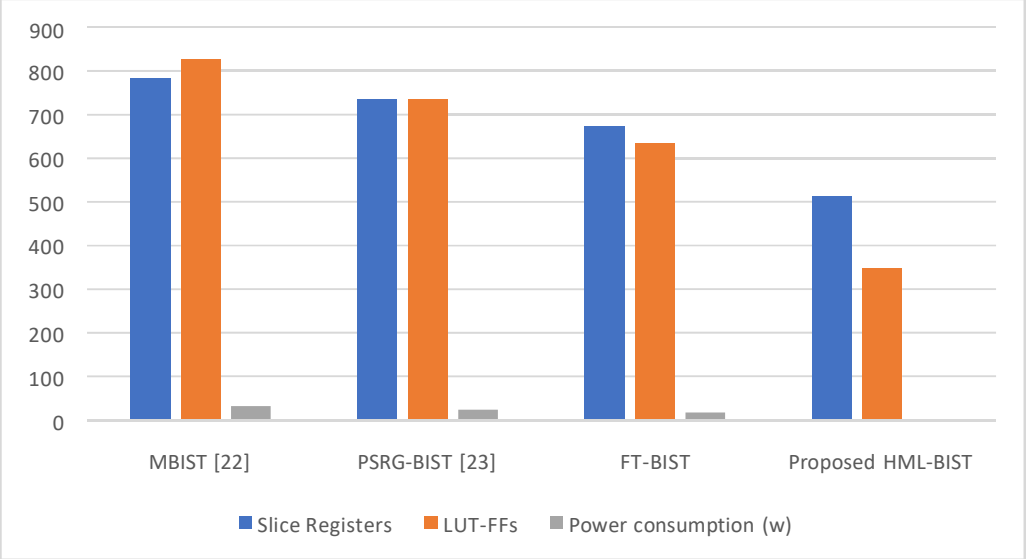

Figure 7.11. Graphical representation of performance evaluation.

CHAPTER-8

CONCLUSION

The implementation of an HML-BIST, which is used to identify and fix defects in memory elements, is the main goal of this work. To create random test patterns for write address, read address, and write data, LFSR modules were initially introduced. In this case, LFSR is utilized to produce non-repeated random numbers using the activity factor. The information in memory is then compared with the information from the original source using a space comparator. The BIST module then fixes the memory for a variety of test situations. The simulations showed that the suggested BIST method outperformed existing approaches in terms of area, latency, and power.

FUTURE SCOPE

In this article, we have covered the numerous components that are included in LBIST and offered an overview of the LBIST architecture. Comparisons are made between the controller algorithms for "MARCH C-," "MARCH A," and "MARCH Y," as well as their respective Verilog implementation modeling and synthesis. Based on the description of the algorithm and the results of the synthesis, it is clear that the 'MARCH A' algorithm has a greater number of states. As a result, the controller that is implemented using the 'MARCH A' algorithm occupies more space, consumes more average power, and is still slower. In contrast, the controller that is implemented using the 'MARCH Y' algorithm requires the fewest number of states; as a result, it has the smallest footprint, uses the least amount of When compared to the MARCH Y method, the MARCH C-' covers greater faults at the expense of a minimal increase in the amount of space required, the average amount of power used, and the amount of delay.

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ANNEXTURE

The submission has been saved!

Submission 2778	
Title	Implementation of Power Binning-based Logic BIST control using activity factor
Paper:	(Sep 20, 08:29 GMT)
Author keywords	Built in self-test linear feedback shift register memory area delay power
Abstract	Built in self-test (BIST) modules are essential devices in various application, which includes microprocessors, microcontroller, multi-core system, and multi-processor systems. The conventional BIST modules are failed to solve the problems presented in various memories, which are affected by the stuck at faults. Therefore, this work is focused on implementation of an Hybrid Memory Logic (HML)-BIST, which is used to detect and correct the errors presented in the memory elements. Initially, linear feedback shift register (LFSR) modules introduced for generating the random test patterns for write address, read address and write data. Here, activity factor is used to generate the non-repeated random numbers from LFSR. Then, the data stored in memory are compared with original source data using space comparator. Finally, the BIST module corrects the memory for various test cases. The simulations revealed that the proposed HML-BIST method resulted in better area, delay, power performance as compared to conventional approaches.
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