A

Course File Report

On

ANALOG AND DIGITAL ELECTRONICS

Submitted by

Mr.S.Sudhakar
Assistant Professor

In the department of
Information Technology (IT)

CMR ENGINEERING COLLEGE
(Approved by AICTE-New Delhi, Affiliated to J.N.T.U, Hyderabad)
Kandlakoya (v), Medchal Road, Hyderabad-501 401, Telangana State, India .Website: www.cmrec.ac.in
(2021-22)

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1. Department vision & mission

VISION

To accomplish an admirable standard of quality education by utilizing the latest technologies, innovations to be applicable for academia and industry which helps society in large.

MISSION

M1: To evolve professional who is proficient in the area of AI-ML

M2: To impart principle-based education and contribute to the innovation of computing and learning-based systems.

M3: Our Endeavour is to try new advancements in high-end computing hardware and software for society

2.List of PEOs, POs, PSOs

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)

Programme educational objectives are broad statements that describe the career and professional accomplishments that the programme is preparing graduates to achieve within 3 to 5 years after graduation.

The **Programme Educational Objectives** of the B. Tech CSE programme are:

PEO1: To apply the knowledge of mathematics, basic science and engineering solving the real world computing problems to succeed higher education and professional careers.

PEO2: To develop the skills required to comprehend, analyze, design and create innovative computing products and solutions for real life problems.

PEO3: To inculcate professional and ethical attitude, communication and teamwork skills, multi-disciplinary approach and an ability to relate computer engineering issues with social awareness

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to satisfy these NBA graduate attributes:

1. **Engineering knowledge:** An ability to apply knowledge of computing, mathematics, science and engineering fundamentals appropriate to the discipline
2. **Problem analysis:** An ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution
3. **Design/development of solutions:** An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs with appropriate consideration for public health and safety, cultural, societal and environmental considerations

4. **Conduct investigations of complex problems:** An ability to design and conduct experiments, as well as to analyze and interpret data
5. **Modern tool usage:** An ability to use current techniques, skills, and modern tools necessary for computing practice
6. **The engineer and society:** An ability to analyze the local and global impact of computing on individuals, organizations, and society
7. **Environment and sustainability:** Knowledge of contemporary issues
8. **Ethics:** An understanding of professional, ethical, legal, security and social issues and responsibilities
9. **Individual and team work:** An ability to function effectively individually and on teams, including diverse and multidisciplinary, to accomplish a common goal
10. **Communication:** An ability to communicate effectively with a range of audiences
11. **Project management and finance:** An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects
12. **Life-long learning:** Recognition of the need for and an ability to engage in continuing professional development

PROGRAM SPECIFIC OUTCOMES (PSO'S)

1. **Professional Skills and Foundations of Software development:** Ability to analyze, design and develop applications by adopting the dynamic nature of Software developments
2. **Applications of Computing and Research Ability:** Ability to use knowledge in cutting edge technologies in identifying research gaps and to render solutions with innovative ideas

3. List of COs (action verbs as per blooms)

CO.1	• Know the characteristics of various components.
CO.2	• Understand the utilization of components.
CO.3	• Design and analyze small signal amplifier circuits.
CO.4	• Learn Postulates of Boolean algebra and to minimize combinational functions
CO.5	• Design and analyze combinational and sequential circuits
CO.6	• Know about the logic families and realization of logic gates

4. Syllabus copy and suggested or reference books

UNIT - I

Diodes and Applications: Junction diode characteristics: Open circuited p-n junction, p-n junction as a rectifier, V-I characteristics, effect of temperature, diode resistance, diffusion capacitance, diode switching times, breakdown diodes, Tunnel diodes, photo diode, LED.

Diode Applications - clipping circuits, comparators, Half wave rectifier, Full wave rectifier, rectifier with capacitor filter.

UNIT - II

BJTs: Transistor characteristics: The junction transistor, transistor as an amplifier, CB, CE, CC

configurations, comparison of transistor configurations, the operating point, self-bias or Emitter bias, bias compensation, thermal runaway and stability, transistor at low frequencies, CE amplifier response, gain bandwidth product, Emitter follower, RC coupled amplifier, two cascaded CE and multi stage CE amplifiers.

UNIT - III

FETs and Digital Circuits: FETs: JFET, V-I characteristics, MOSFET, low frequency CS and CD amplifiers, CS and CD amplifiers.

Digital Circuits: Digital (binary) operations of a system, OR gate, AND gate, NOT, EXCLUSIVE OR gate, De Morgan Laws, NAND and NOR DTL gates, modified DTL gates, HTL and TTL gates, output stages, RTL and DCTL, CMOS, Comparison of logic families.

UNIT - IV

Combinational Logic Circuits: Basic Theorems and Properties of Boolean Algebra, Canonical and Standard Forms, Digital Logic Gates, The Map Method, Product-of-Sums Simplification, Don’t-Care Conditions, NAND and NOR Implementation, Exclusive-OR Function, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.

UNIT - V

Sequential Logic Circuits: Sequential Circuits, Storage Elements: Latches and flip flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Shift Registers, Ripple Counters, Synchronous Counters, Random-Access Memory, Read-Only Memory

TEXT BOOKS:

1. Integrated Electronics: Analog and Digital Circuits and Systems, 2/e, Jaccob Millman, Christos Halkias and Chethan D. Parikh, Tata McGraw-Hill Education, India, 2010.
2. Digital Design, 5/e, Morris Mano and Michael D. Cilette, Pearson, 2011.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, Jimmy J Cathey, Schaum's outline series, 1988.
2. Digital Principles, 3/e, Roger L. Tokheim, Schaum's outline series, 1994

5. Session plan/ lesson plan

S.NO	TOPIC TO BE COVERED	Suggested Books (Eg: T1,T2,)	NO. OF LECTURES REQUIRED	Teaching methods
	UNIT-I Classes required - 12			
1	Introduction	T1,R1	1	White board, PPT
2	Junction diode characteristics: Open circuited p-n junction,:	T1	1	White board, PPT
3	V-I characteristics	T1,R1	1	White board, PPT
4	Effect of temperature, diode resistance, diffusion capacitance	T1	2	White board, PPT
5	diode switching times	T1,R1	1	White board, PPT
6	Breakdown diodes ,Tunnel diodes, photo diode, LED	T1	1	White board, PPT
7	Diode Applications - clipping circuits	T1,R1	1	White board, PPT
8	Comparators	T1	1	White board, PPT
9	Half wave rectifier, Full wave rectifier	T1	2	White board, PPT
10	capacitor filter	T1	1	White board, PPT

Unit-II Classes required-13				
11	**BJTs**: Transistor characteristics: The junction transistor	**T1,R1**	**2**	**White board, PPT**
12	transistor as an amplifier	**T1**	**2**	**White board, PPT**
13	CB configurations, CE configurations	**T1**	**1**	**White board, PPT**
14	CC configurations, comparison of transistor configurations	**T1**	**1**	**White board, PPT**
15	the operating point, self-bias or Emitter bias, bias compensation	**T1**	**1**	**White board, PPT**
16	Thermal runaway and stability	**T1**	**1**	**White board, PPT**
17	Transistor at low frequencies, CE amplifier Response	**T1**	**1**	**White board, PPT**
18	Gain bandwidth product	**T1**	**1**	**White board, PPT**
19	Emitter follower, RC coupled amplifier	**T1**	**2**	**White board, PPT**
20	two cascaded CE and multi stage CE amplifiers	**T1**	**1**	**White board, PPT**
UNIT-III Classes required - 10				
21	**FETs and Digital Circuits**: FETs: JFET, V-I characteristics	**T1**	**1**	**White board, PPT**
22	MOSFET	**T1**	**1**	**White board, PPT**
23	low frequency CS and CDamplifiers	**T1**	**1**	**White board, PPT**
24	Digital Circuits: Digital (binary) operations of a	**T1**	**1**	**White board, PPT**

	system,			
25	OR gate, AND gate, NOT, EXCLUSIVE OR Gate	**T1**	**1**	**White board, PPT**
26	De Morgan Laws	**T1**	**1**	**White board, PPT**
27	NAND and NOR DTL gates	**T1**	**1**	**White board, PPT**
28	modified DTL gates	**T1**	**1**	**White board, PPT**
29	HTL and TTL gates output stages, RTL and DCTL,	**T1**	**1**	**White board, PPT**
30	CMOS, Comparison of logic families	**T1**	**1**	**White board, PPT**
UNIT-IV Classes required - 10				
31	**Combinational Logic Circuits:** Basic Theorems and Properties of Boolean Algebra,	**T2**	**1**	**White board, PPT**
32	Canonical and Standard Forms, Digital Logic Gates	**T2**	**1**	**White board, PPT**
33	The Map Method, Product-of-Sums Simplification, Don't-Care Conditions	**T2**	**1**	**White board, PPT**
34	NAND and NOR Implementation	**T2**	**2**	**White board, PPT**
35	Exclusive-OR Function	**T2**	**1**	**White board, PPT**
36	Binary Adder-Subtractor, Decimal Adder	**T2**	**1**	**White board, PPT**
37	Binary Multiplier	**T2**	**1**	**White board, PPT**
38	Magnitude Comparator	**T2**	**1**	**White board, PPT**

39	Decoders, Encoders, Multiplexers	**T2**	**2**	**White board, PPT**
UNIT-V Classes required - 12				
40	**Sequential Logic Circuits:** Sequential Circuits,	**T2**	1	**White board, PPT**
41	Storage Elements: Latches and flip flops	**T2**	2	**White board, PPT**
42	Analysis of Clocked Sequential Circuits	**T2**	1	**White board, PPT**
43	State Reduction and Assignment	**T2**	2	**White board, PPT**
44	Shift Registers	**T2**	2	**White board, PPT**
45	Ripple Counters	**T2**	2	**White board, PPT**
46	Synchronous Counters	**T2**	2	**White board, PPT**
Total no of classes : 57				

Individual Time Table

	I	II	III	IV		V	VI	VII
MON	ADE-A		ADE-B					
TUE		ADE-B				ADE- A		
WED								
THU		ADE-B		ADE-A				ADE-B
FRI	ADE-B		ADE-A					
SAT							ADE-B	

6. Session execution log

S NO	UNIT	SCHEDULED COMPLETED DATE	COMPLETED DATE	REMARKS
1	I	06.09.2021	07.10.2021	Completed
2	II	08.10.2021	3.11.2021	Completed
3	III	15.11.2021	7.12.2021	Completed
4	IV	09.12.2021	24.12.2021	Completed
5	V	27.12.2021	07.01.2022	Completed

7. Lecture notes

ADE NOTES.rar

8. Assignment Questions along with sample assignment

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Mid-I Assignment Questions

MID – I ASSIGNMENT

IT II- I (2021 – 2022)

ANALOG AND DIGITAL ELECTRONICS

1) (A)Explain Biasing Modes Of P-N Junction Diode ?(C01)
   (B)Explain Diode Switching Times?
2) (A)Describe About Break Down Mechanism?
   (B)Explain About Zener Diode And Avalanche Diodes (Co1)
3) (A)Explain About Ce Configuration Of Transistor?
   (B)Compare Transistor Three Configurations (Co2)
4) Explain About Transistor Operating Point?(Co2)
5) Explain Full Wave Rectifier And Its Efficiency?(Co1)
6) Explain Diffusion Capacitance And Diode Resistance ?(Co1)
7) Explain About These Following Diodes A)Tunnel Diode B) Photo Diode ?(Co2)
8) Explain About Self Bias Or Emitter Bias Of A Transistor ? (Co2)

9) Explain About Thermal Stability And Thermal Runaway?
10) What Is Early Effect And Punch Through Effect?

Innovative Questions

11) Why Inverse Active Mode Of Transistor Is Not Useful?(Co2)
12) Zener Diode As Voltage Regulator(Co1)

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Mid-II Assignment Questions

IT II- I (2021 – 2022)
MID – II ASSIGNMENT

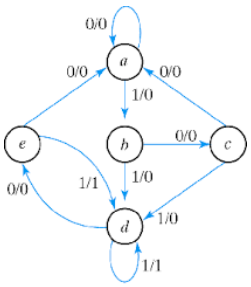
ANALOG AND DIGITAL ELECTRONICS

1. A) Explain the realization of SR flip-flop, JK flip-flop and D flip-flop (CO5)
   B) Compare LATCHES and FLIP FLOPS? (CO5)
2. A) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates. (CO4)
   B) Minimize the following expressions using K-map and realize using NAND Gates. f = ∑m (1, 3, 5, 8, 9, 11, 15) +d (2, 13). (CO4)
3. A) How do you obtain dual of an expression?
   B) What are canonical and standard forms of an expressions (CO4)
   C) Simplify the following Boolean expressions using the Boolean theorems. (CO4)
   (i) (A+B+C) (B□+C) + (A+D) (A□+C) (ii) (A+B) (A+B□) (A□+B)
4. A) Explain about 4 bit magnitude comparator?(CO5)
   B) Explain about priority encoder? (CO5)
   C) Design a full adder using two half adders? (CO5)

5. A) What is ripple counter? Explain modulo-8 ripple counter? (CO6)
   B) What are different types of shift registers? (CO6)
   C) Difference between synchronous and asynchronous circuits? (CO6)

6. A) Explain about all types of RAM and ROM(CO6)
   B) Explain about 8*1 multiplexer (CO5)
   C) Explain about 1*4 demultiplexer? (CO5)

7. A) Obtain reduce state table and reduce state diagram for the sequential machine whose state diagram is shown in the figure. (CO6)



B) Difference between combinational and sequential circuits ? (CO5)

8 A) Compare FET and BJT? (CO3)

B) Draw HTL and TTL gates? (CO3)

C) Explain about modified DTL gates? (CO3)

9. A) COMPARE ALL logic families (CO3)

B) Explain the operation of Depletion mode MOSFET in detail(CO3)

10. A) Simplify the following expressions and implement them with NAND gate circuits. (CO4)

(i) F=AB'+ABD+ABD'+A'C'D'+A'BC' (ii) G=BD+BCD'+AB'C'D'

B) Express the following as the sum of minterms and product of maxterms. (CO4)

i)F(A,B,C,D)=B'D+A'D+BD

ii)F(X,Y,Z)=(XY+Z)(XZ+Y)

INNOVATIVE QUESTIONS

13) Prove that OR-AND logic network is equivalent to NOR –NOR network ?(CO4**)**

14) Design gray code using binary code ? (CO5)

9. Mid exam question papers along with sample answer scripts.

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II.B.TECH- I-SEM -I MID EXAMINATIONS, ***Date:*** **8/11/2021**
Time*: 10.AM TO 11.30 AM*

Subject: ADE **Branch:IT** **Marks: 25 M**

Note: Question paper contains two parts,Part - A and Part - B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B consists of (21/2) units. Answer any one full question from each unit. Each question carries

5 marks and may have a,b,c sub questions.

PART-A **5x2=10**

1.Plot the V-I characteristics of p-n junction diode?

2.What is the effect of temperature on diodes?

3.What is Thermal runaway of transistor?

4.Operating regions of transistor?

5.What is early effect and punch through effect?

PART-B **3X5=15**

6.Descibe the following diodes

(a) Tunnel diode

(b) Photodiode

(or)

7.explain about the following breakdown mechanisms?

(a) Avalanche breakdown mechanisms

(b) Zener Diode breakdown mechanisms

8.(a) Explain operating point of transistor?

(b) How transistor acts as an amplifier?

(or)

9.(a) Compare CE,CC,CB configurations of transistor?

(b) Relation among α,β,ϒ?

10.(a) Self bias of transistor (or) voltage divider biasing method of a transistor?

(b) Define stability factors for s, s^1 ?

(or)

11.(a) Define Full wave rectifier and its efficiency?

(b) Define Diode switching times?

II.B.TECH- I-SEM -II MID EXAMINATIONS, ***Date:*** **7/1/2022**

Time*: 10AM TO 11.30 AM*

Subject: ADE **Branch: IT** **Marks: 25 M**

Note: Question paper contains two parts,Part - A and Part - B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B consists of (21/2) units. Answer any one full question from each unit. Each question carries

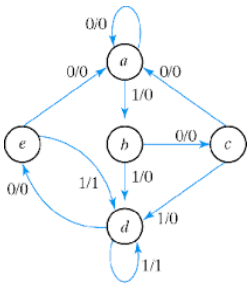
5 marks and may have a,b,c sub questions.

PART-A **5x2=10**

1. Compare LATCHES and FLIP FLOPS? (CO5)?
2. Difference between synchronous and asynchronous circuits? (CO6)
3. Difference between combinational and sequential circuits? (CO5)
4. COMPARE ALL logic families (CO3)?
5. Explain about all types of RAM and ROM? (CO6)

PART-B **3X5=15**

6. A) Obtain reduce state table and reduce state diagram for the sequential machine whose state diagram is shown in the figure. (CO6)



B) Explain about priority encoder? (CO5)

(or)

7. A) What are canonical and standard forms of an expressions (CO4)

B) Simplify the following Boolean expressions using the Boolean theorems. (CO4)
(i) (A+B+C) (B□+C) + (A+D) (A□+C) (ii) (A+B) (A+B□) (A□+B)

8 A) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates. (CO4)

B) Minimize the following expressions using K-map and realize using NAND Gates.

f = ∑m (1, 3, 5, 8, 9, 11, 15) +d (2, 13). (CO4)

(or)

9. A) What is ripple counter? Explain modulo-8 ripple counter? (CO6)

B) What are different types of shift registers? (CO6)

10. A) Compare FET and BJT? (CO3)?

B) Explain the operation of Depletion mode MOSFET in detail? (CO3)

(or)

11. A) Design a full adder using two half adders? (CO5)

B) Explain about 8*1 multiplexer and 3*8 Decoder (CO5)

SET 2

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II.B.TECH- I-SEM -II MID EXAMINATIONS, *Date:* Time*:*

Subject: ADE Branch: IT Marks: 25 M

Note: Question paper contains two parts, Part – A and Part - B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B consists of (21/2) units. Answer any one full question from each unit. Each question carries

5 marks and may have a,b,c sub questions.

PART-A **5x2=10**

7. State different types of FLIP FLOPS? (CO6)?
8. Difference between synchronous and asynchronous counters? (CO6)
9. Explain about shift registers ? (CO5)
10. What is state assignment? Explain with a suitable example (CO3)?
11. Explain about encoders and decoders (CO4)

PART-B **3X5=15**

12. A) Obtain reduce state table and reduce state diagram for the sequential machine whose state table is shown in the figure. (CO6)

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

B) design 16*4 encoder by using two 8*3 encoders (CO5)

(or)

7. A) What are canonical and standard forms of an expressions (CO4)

   B) Explain the working of 2 bit magnitude comparator ? (CO4)

8 A) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates. (CO4)

B) Minimize the following expressions using K-map and realize using NOR Gates.

$f = \sum m (1, 3, 5, 7,8, 9,10, 11,12,14, 15) + d (2, 4,13)$. (CO4)

(or)

9. A) What is Asynchronous counter? Explain modulo-8 Asynchronous counter? (CO6)

B) Define memory ? classifications of memories ?(CO6)

10. A) Compare JFET and MOSFET? (CO3)?

B) Explain the operation of JFET in detail? (CO3)

(or)

11. A) Design a full subtractor using two half subtractors? (CO4)

B) State Demorgan's laws? prove it (CO4)

SET 3

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II.B.TECH- I-SEM -II MID EXAMINATIONS, *Date:* Time*:*

Subject: ADE Branch: IT Marks: 25 M

Note: Question paper contains two parts, Part – A and Part - B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B consists of (21/2) units. Answer any one full question from each unit. Each question carries

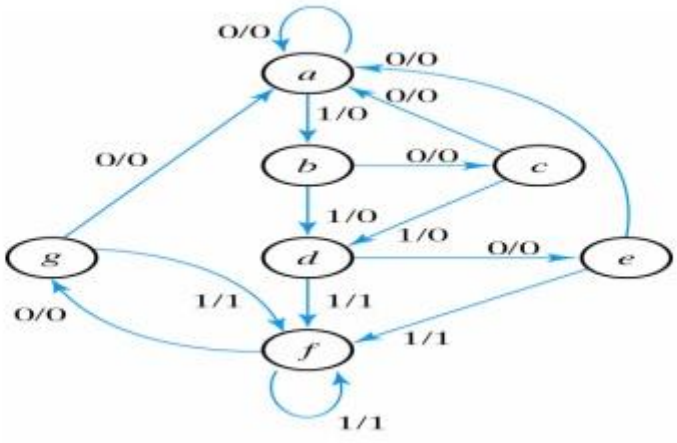
5 marks and may have a,b,c sub questions.

PART-A 5x2=10

13. Implement AND gate using TTL logic? (CO3)?
14. Write a logic of full adder with Boolean equations? (CO4)
15. Define D flip flop with the help of its characteristics equations ? (CO5)
16. What is BCD adder? (CO4)?
17. What is race around condition? how it is eliminated ? (CO6)

PART-B 3X5=15

18. A) Obtain reduce state table and reduce state diagram for the sequential machine whose state diagram is shown in the figure. (CO6)



B) what is priority encoder ?Explain (CO4)

(or)

7. A) Minimize the following expressions using K-map and realize using NOR Gates.

$f = \sum m (1, 3, 4,11,12,13,14,15)$ (CO4)

B) Design SR flip flop using NOR gates ? (CO5)

8 A) $(A^1 B^1 C^1) + (A B^1 C^{1)} + (A^1 B^1 C) + (A BC^1) + (A^1 BC)$

Reduce the following expression , and draw circuit diagram using AND-OR-INVETER logic. (CO4)

B) Minimize the following expressions using K-map and realize using NOR Gates.

$f = \pi M(1, 3, 5, 7, 8, 9, 10, 11, 12,14, 15) + d (2, 4,13)$. (CO4)

(or)

9. A) Compare all logic families ? (CO3)

B) Draw different types of logic gates and state its truth tables ?(CO4)

10. A) Explain operation of JFET common source configuration (CO3)?

B) Explain the operation of CMOS in detail ? Design a CMOS NAND gate (CO3)

(or)

11. A) state and prove the laws of Boolean Algebra ? (CO4)

B)Explain operation of Master –slave JK flip flop (CO6)

10. Scheme of evaluation

Scheme of Evaluation(MID-1)

S.No	Theory(Part-A)	Marks	Total
1	Plot the V-I characteristics of p-n junction diode?	2M	**2M**
2	What is the effect of temperature on diodes?	2M	**2M**
3	What is Thermal runaway of transistor?	2M	**2M**
4	Operating regions of transistor?	2M	**2M**
5	What is early effect	1M	**2M**
	What is punch through effect?	1M	
Total			**10M**

S.No	Theory(Part-B)	Marks	Total
6	Descibe the following diodes (a) Tunnel diode	2 1/2M	**5M**
	(b) Photodiode	2 1/2M	
7	Explain about the following breakdown mechanisms? (a) Avalanche breakdown mechanisms	2 1/2M	**5M**
	(b) Zener Diode breakdown mechanisms	2 1/2M	
8	8.(a) Explain operating point of transistor?	2 1/2M	**5M**
	(b) How transistor acts as an amplifier?	2 1/2M	
9	(a) Compare CE,CC,CB configurations of transistor?	2 1/2M	**5M**
	(b) Relation among α,β,ϒ?	2 1/2M	
5.	(a) Self bias of transistor (or) voltage divider biasing method of a transistor?	2 1/2M	**5M**

	(b) Define stability factors for s, s^1 ?	FOR S DERIVATION (1) FOR s^1 DERIVATION (1 1/2M)	
6.	(a) Define Full wave rectifier and its efficiency?	2 1/2M	**5M**
	(b) Define Diode switching times?	2 1/2M	

Scheme of Evaluation (MID-2)

S.No	Theory(Part-A)	Marks	Total
1	Compare LATCHES and FLIP FLOPS?	2M	**2M**
2	Difference between synchronous and asynchronous circuits?	2M	**2M**
3	Difference between combinational and sequential circuits?	2M	**2M**
4	COMPARE ALL logic families	2M	**2M**
5	Explain about RAM	1M	**2M**
	Explain about ROM	1M	
Total			**10M**

S.No	Theory(Part-B)	Marks	Total
6	a) Obtain reduce state table	1 M	**5M**
	Obtain reduce state diagram	1 1/2M	
	(b) Explain about priority encoder explanation	1 1/2M	
	Block Diagram	1 M	
7	a) What are canonical forms of an expressions	1 M	**5M**
	What are standard forms of an expressions	1 M	
	(b) Simplify the following Boolean expressions using the Boolean theorems. (i) (A+B+C) (B□+C) + (A+D) (A□+C)	1 1/2M	

	(ii) (A+B) (A+B□) (A□+B)	1 1/2M	
8	(a) Why a NAND and NOR gates are known as universal gates?	1 M	**5M**
	Simulate all the basic Gates	1 1/2M	
	(b) Minimize the following expressions using K-map and. f = ∑m (1, 3, 5, 8, 9, 11, 15) +d (2, 13).	1 M	
	realize using NAND Gates	1 1/2M	
9	(a) What is ripple counter?	1 M	
	Explain modulo-8 ripple counter?	1 1/2M	
	(b) What are different types of shift registers	2 1/2M	**5M**
10.	(a) Compare FET and BJT?	2 1/2M	**5M**
	(b) Explain the operation of Depletion mode MOSFET in detail		
	Operation	1M	
	Diagram	1 1/2M	
11.	(a) Design a full adder using two half adders?	2 1/2M	**5M**
	(b)) Explain about 8*1 multiplexer	1 1/2M	
	Explain about 3*8 Decoder?	1 M	

11.Mapping of COs with POs and PSOs

COURSE CO-PO&PSO-MATRIX	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	-	2	-	-	-	-	-	-	1	1	-
CO2	3	3	3	3	3	3	-	-	-	-	-	1	1	1
CO3	3	3	3	2	2	2	-	-	-	-	-	1	1	-

CO4	3	3	3	2	2	2	-	-	-	-	-	1	1	1
CO5	3	3	3	2	2	2	-	-	-	-	-	1	1	-
C06	3	3	3	2	2	2	-	-	-	-	-	2	1	1
AVERAGE	**3**	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

12.Attainment of COs with POs and PSOs

Relationship of Course outcomes to Program Outcomes (PO AVG)													
PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**

ASSESSMENT OF POs THROUGH THE COURSE			
PO	**CO**	**Value**	**AVG PO (Mid)**
PO1	CO1		
	CO3		
	CO4		
	CO5		
	CO6		
PO2	CO1		
	CO2		
	CO3		
	CO4		
	CO5		
PO3	CO1		
	CO2		
	CO3		
	CO4		
	CO5		
	CO6		
PO4	CO2		
	CO3		

	CO6		
PO5	CO5		
PO12	CO2		
PSO1	CO2		
	CO3		
PSO2	CO1		
	CO2		
	CO3		
	CO4		
	CO6		

13. University question papers or question bank.

ADE JNTUH QUESTION PAPERS.rar

QUESTION BANK

ANALOG AND DIGITAL ELECTRONICS question bank.zip

14.Power point presentations

ade unit 1.zip

ade unit 2.zip

ADE 3 UNIT.zip

ade 4th unit.zip

ADE 5TH UNIT.zip

15. Websites or URLs e- Resources

1. nptel.ac.in/courses/108/102/108102095/
2. nptel.ac.in/courses/108/105/108105132/
3. nptel.ac.in/courses/108/102/108102112/
4. www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
5. https://www.coursera.org/specializations/semiconductor-devices