Analog Multiplier and PLL

UNIT–III

Introduction

- Nonlinear operations on continuous-valued analog signals are often required in instrumentation, communication, and control-system design.
- These operations include
  - rectification,
  - modulation,
  - demodulation,
  - frequency translation,
  - multiplication, and
  - division.
- In this chapter we analyze the most commonly used techniques for performing multiplication and division within a monolithic integrated circuit

Introduction

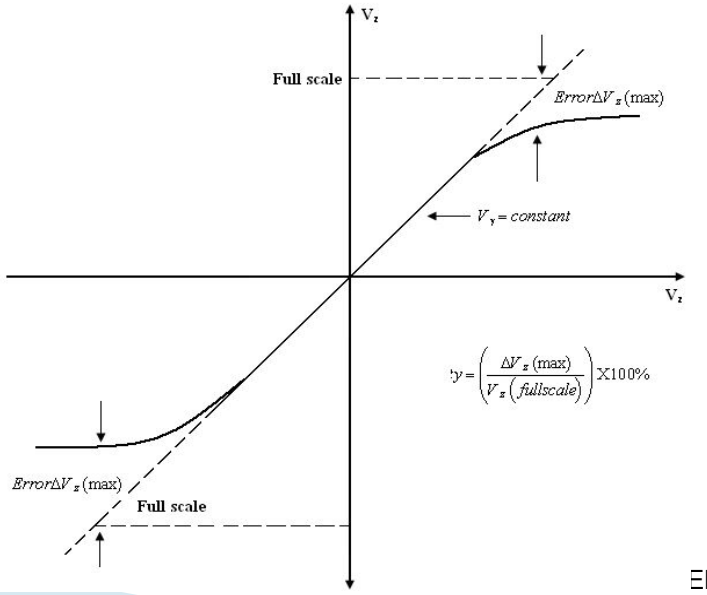
- In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product.
- Such circuits are termed *analog multipliers*.
- In the following sections we examine several analog multipliers that depend on the exponential transfer function of bipolar transistors .

MULTIPLIERS

- A multiple produces an output V0 , which is proportional to the product of two inputs Vx and Vy.
  That is, V0 = K Vx Vy
- where K is the scaling factor that is usually maintained as (1/10) V-1
- There are various methods available for performing analog multiplication. Four of such techniques, namely,
- 1. Logarithmic summing technique
  2. Pulse height/width modulation Technique
  3. Variable trans conductance Technique
  4. Multiplication using Gilbert cell and
  5. Multiplication using variable trans conductance technique.

Terminologies associated voltage of the multiplier characteristics

- **Accuracy:**
  This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.
- **Linearity:**
  This defines the accuracy of the multiplier. It represents the maximum percentage derivation from the ideal straight line output. An error surface is formed by plotting the output for different combinations of X and Y inputs. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.



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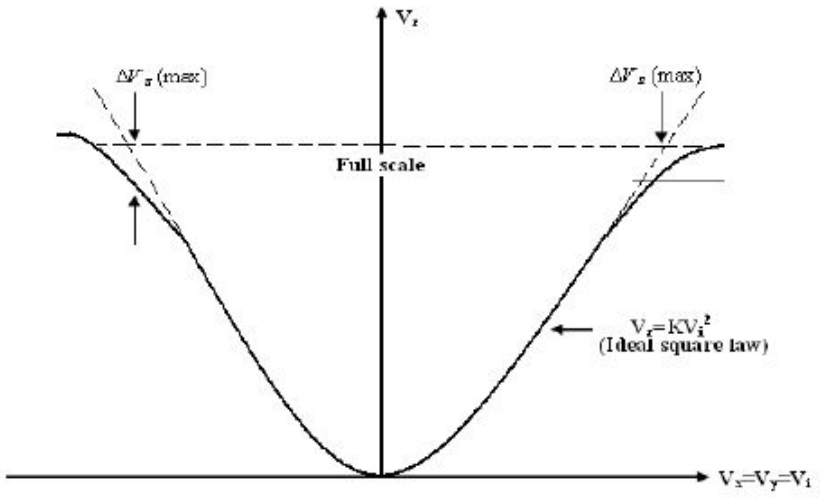
- **Squaring Mode Accuracy:**
  The Square – law curve is obtained with both the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square – law curve expresses the squaring mode accuracy.



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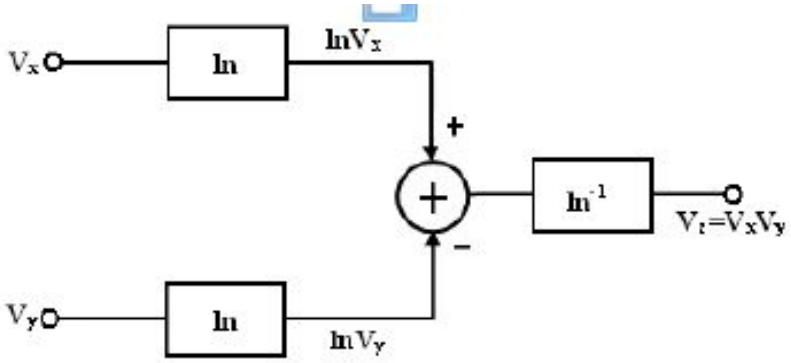
Bandwidth:
The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.
The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristics defines the application frequency ranges when used for phase detection or AM detection.
Quadrant:
The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four

Logarithmic summing Technique:

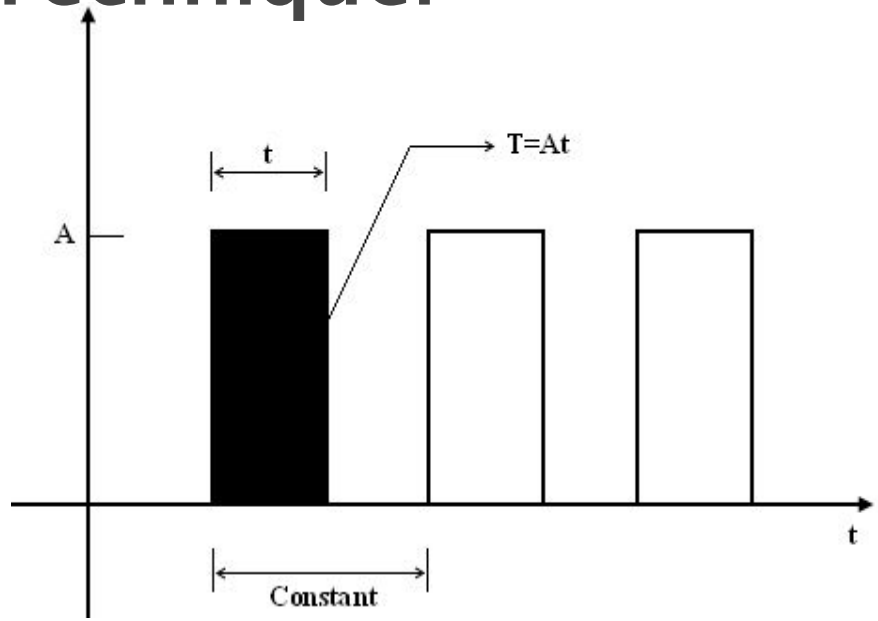
- This technique uses the relationship
  lnVx + lnVy =ln(VxVy)



➢Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of Vx and Vy.

➢ this type of multiplier is restricted to one quadrant operation only.

Pulse Height/ Width Modulation Technique:



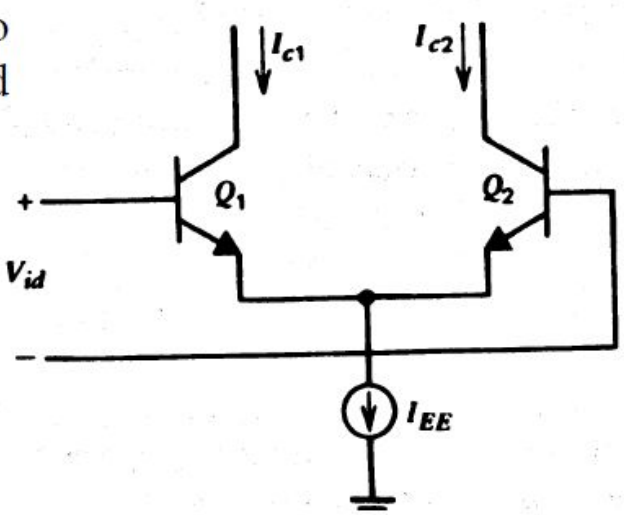
$$V_z = K_z T = K_z At = V_x V_y / K_x K$$

Multiplier using Emitter coupled Transistor pair

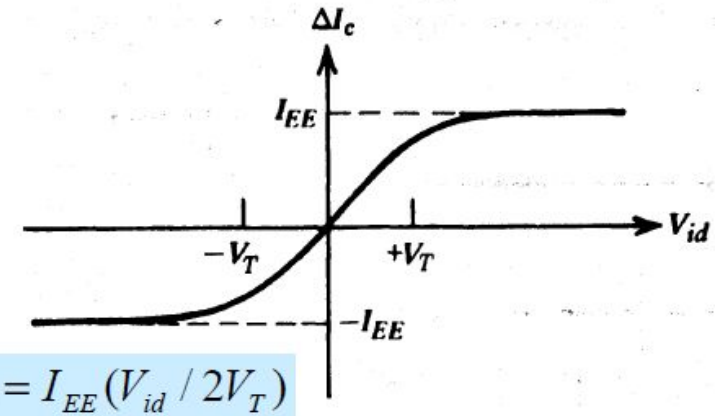
- The emitter-coupled pair, was shown in to produce output currents that were related to the differential input voltage by :

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)} \qquad I_{c2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$$

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE}\tanh(V_{id}/2V_T)$$



- This relationship is plotted => and shows that the emitter-coupled pair by itself can be used as a primitive multiplier.



or assuming $(V_{id}/2V_T) << 1, \Rightarrow \Delta I_c = I_{EE}(V_{id}/2V_T)$

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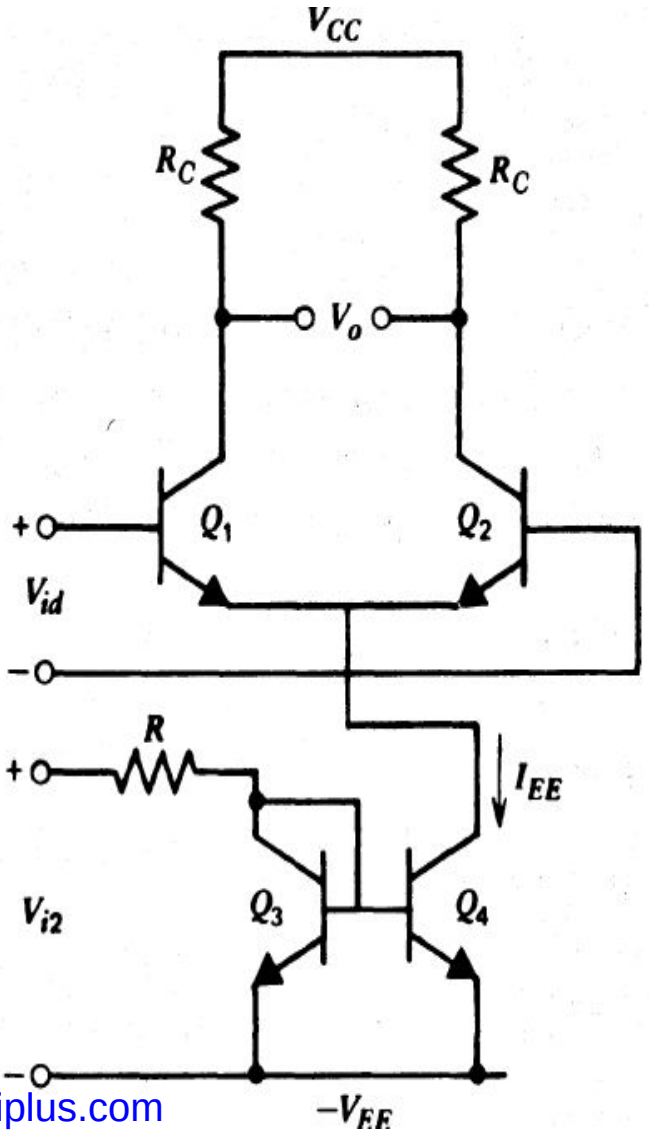
- The current I_{EE} is actually the bias current for the emitter-coupled pair.
- With the addition of more circuitry, we can make I_{EE} proportional to a second input signal.
- Thus we have

$$I_{EE} \cong K_o(V_{i2} - V_{BE(on)})$$

- The differential output current of the emitter-coupled pair can be calculated to give

$$\Delta I_c \cong \frac{K_o V_{id}(V_{i2} - V_{BE(on)})}{2V_T}$$

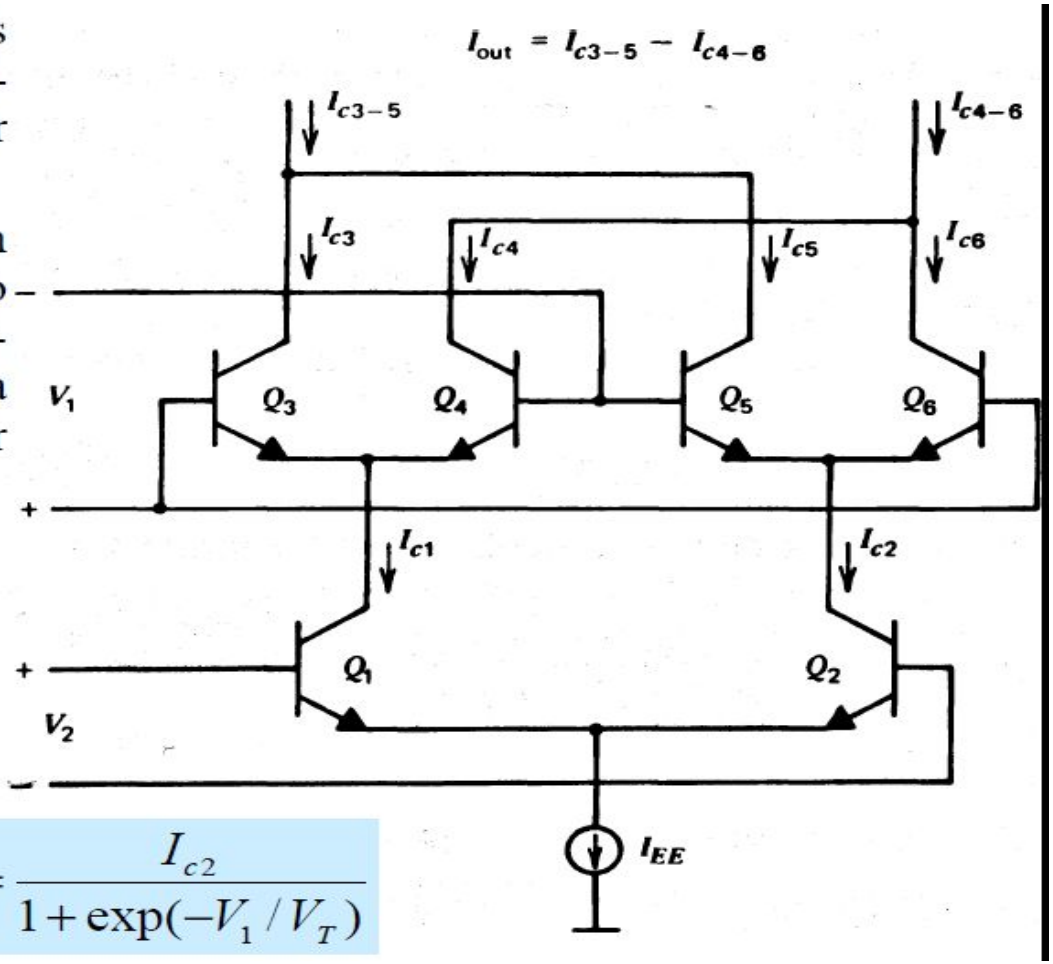


Two-Quadrant restriction

- Thus we have produced a circuit that functions as a multiplier under the assumption that *Vid* is small, and that *Vi2* is greater than $V_{BE(on)}$.
- The latter restriction means that the multiplier functions in only two quadrants of the *Vid* - *Vi2* plane, and this type of circuit is termed a two-quadrant multiplier.
- The restriction to two quadrants of operation is a severe one for many communications applications, and most practical multipliers allow four-quadrant operation.
- The Gilbert multiplier cell, shown, is a modification of the emitter-coupled cell, which allows four-quadrant multiplication.

Gilbert multiplier cell

- The Gilbert multiplier cell is the basis for most integrated-circuit balanced multiplier systems.
- The series connection of an emitter-coupled pair with two cross-coupled, emitter-coupled pairs produces a particularly useful transfer characteristic,.



$$I_{c3} = \frac{I_{c1}}{1+\exp(-V_1/V_T)}$$

$$I_{c4} = \frac{I_{c1}}{1+\exp(V_1/V_T)}$$

$$I_{c5} = \frac{I_{c2}}{1+\exp(V_1/V_T)}$$

$$I_{c6} = \frac{I_{c2}}{1+\exp(-V_1/V_T)}$$

- The two currents I_{c1} and I_{c2} are related to V2

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_2/V_T)} \qquad I_{c2} = \frac{I_{EE}}{1+\exp(V_2/V_T)}$$

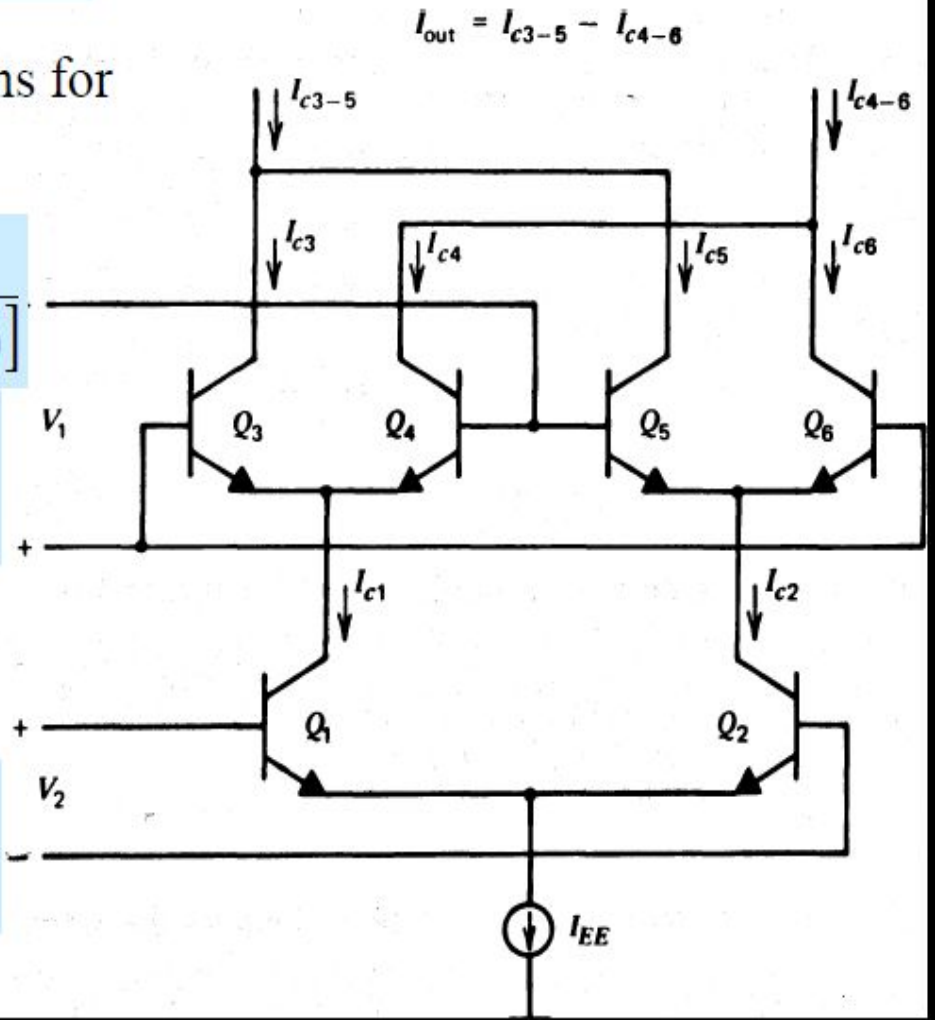
- Substituting I_{c1} and I_{c2} in expressions for
- I_{c3} , I_{c4}, I_{c5} and I_{c6} get :

$$I_{c3} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c4} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c5} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(V_2/V_T)]}$$

$$I_{c6} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(V_2/V_T)]}$$



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- The differential output current is then given by

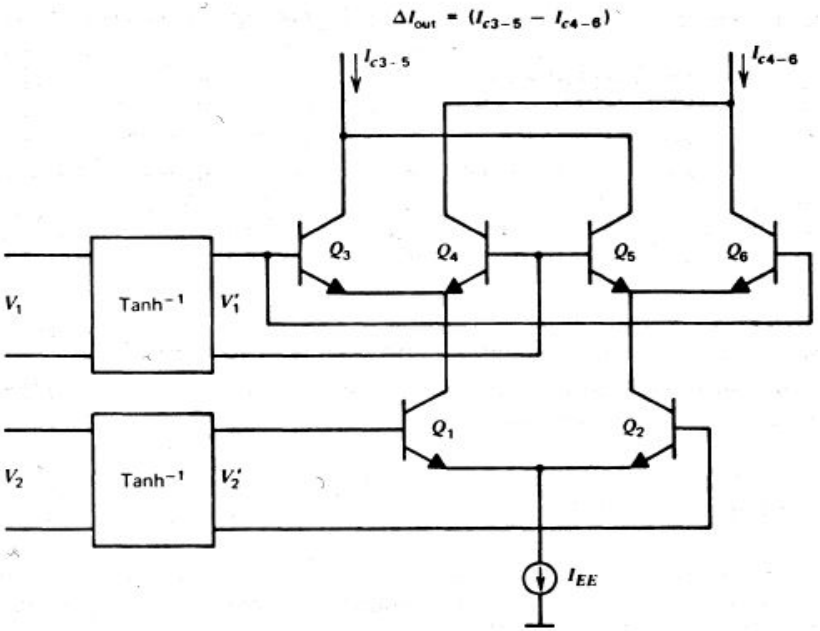
$$\Delta I = I_{c3-5} - I_{c4-6} = I_{c3} + I_{c5} - (I_{c4} + I_{c6}) = (I_{c3} - I_{c6}) - (I_{c4} - I_{c5}) =$$
$$= I_{EE} \tanh(V_1 / 2V_T) \tanh(V_2 / 2V_T)$$

- The dc transfer characteristic, then, is the product of the hyperbolic tangent of the two input voltages. The are three main application of Gilbert cell depending of the V1 an V2 range:
- (1) If $V_1 < V_T$ and $V_2 < V_T$ then : $\tanh(V_{1,2} / 2V_T) \cong V_{1,2} / 2V_T$ and it woks as multiplier
- (2) If one of the inputs of a signal that is large compared to V_T, this effectively multiplies the applied small signal by a square wave, and acts as a modulator.
- (3) If both inputs are large compared to V_T, and all six transistors in the circuit behave as nonsaturating switches. This is useful for the detection of phase differences between two amplitude-limited signals, as is required in phase-locked loops, and is sometimes called the phase-detector mode.

Gilbert cell as Multiplier

(1) If $V_1 < V_T$ and $V_2 < V_T$ then : $\tanh(x) = x + x^3/3 + ... \cong x$

- Thus for small-amplitude signals, the circuit performs an analog multiplication. Unfortunately, the amplitudes of the input signals are often much larger than V_T
- An alternate approach is to introduce a nonlinearity that predistorts the input signals to compensate for the hyperbolic tangent transfer characteristic of the basic cell.
- The required nonlinearity is an inverse hyperbolic tangent characteristic



Pre-warping circuit - inverse hyperbolic tangent

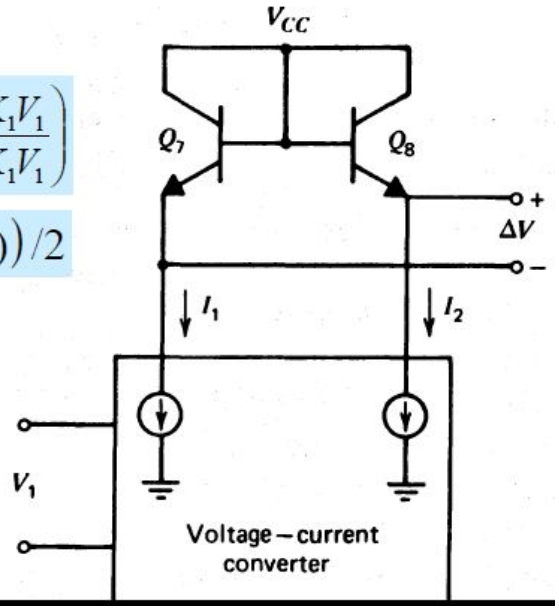
- We assume for the time being that the circuitry within the box develops a differential output current that is linearly related to the input voltage 7i. Thus

$$I_1 = I_{o1} + K_1 V_1 \text{ and } I_2 = I_{o1} - K_1 V_1$$

- Here I_{o1} is the dc current that flows in each output lead if $V1$ is equal to zero, and K1 is the transconductance of the voltage-to-current converter
- The differential voltage developed across the two diode-connected transistors is

$$\Delta V = V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_s}\right) - V_T \ln\left(\frac{I_{o1} - K_1 V_1}{I_s}\right) = V_T \ln\left(\frac{I_{o1} + K_1 V_1}{I_{o1} - K_1 V_1}\right)$$

- Using the identity: $\tanh^{-1} x = \ln\left((1+x)/(1-x)\right)/2$
- We get $\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1 V_1}{I_{o1}}\right)$
- And finally $\Delta I = I_{EE}\left(\frac{K_1 V_1}{I_{o1}}\right)\left(\frac{K_2 V_2}{I_{o2}}\right)$



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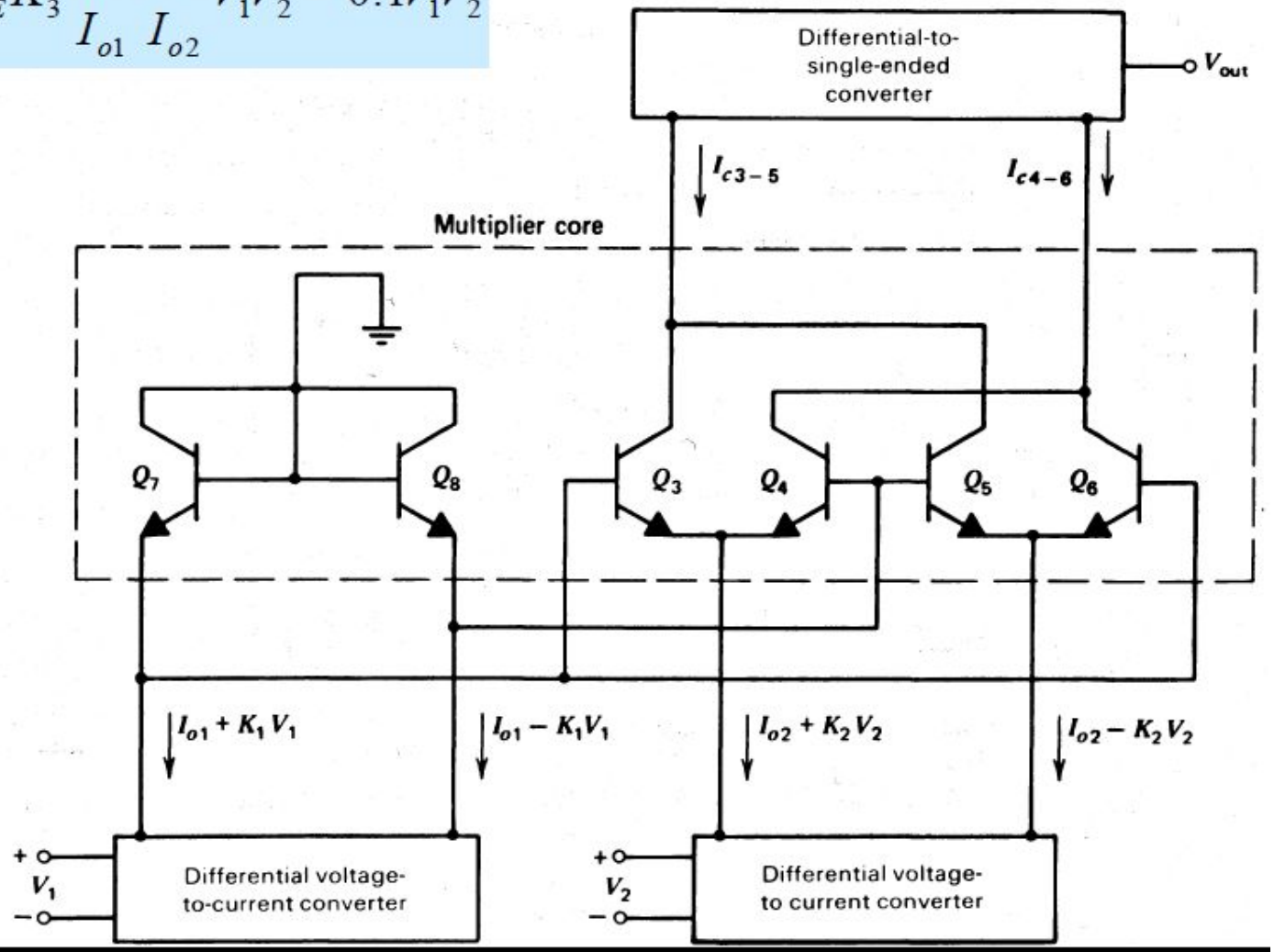
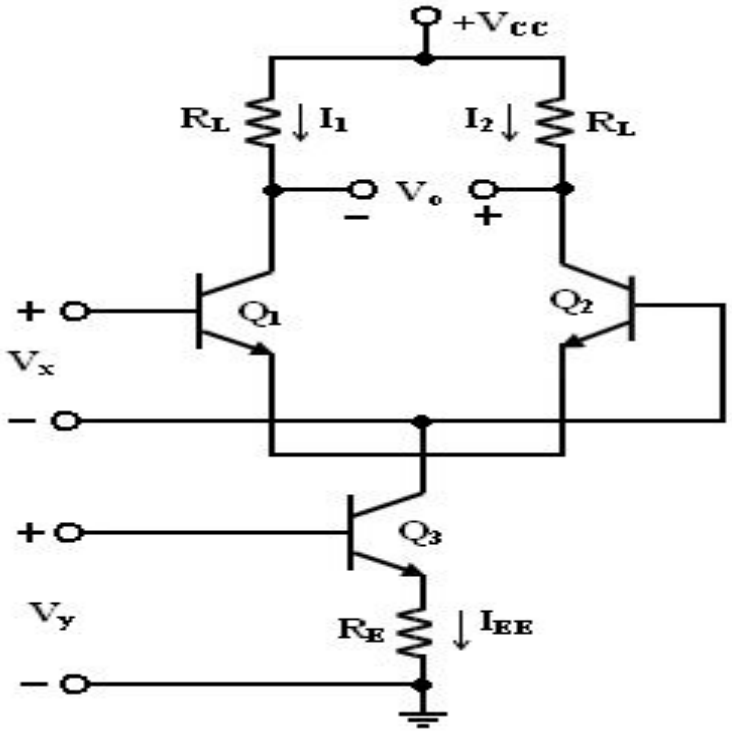
Complete Analog Multiplier

$$V_{out} = I_{EE} K_3 \frac{K_1}{I_{o1}} \frac{K_2}{I_{o2}} V_1 V_2 = 0.1 V_1 V_2$$



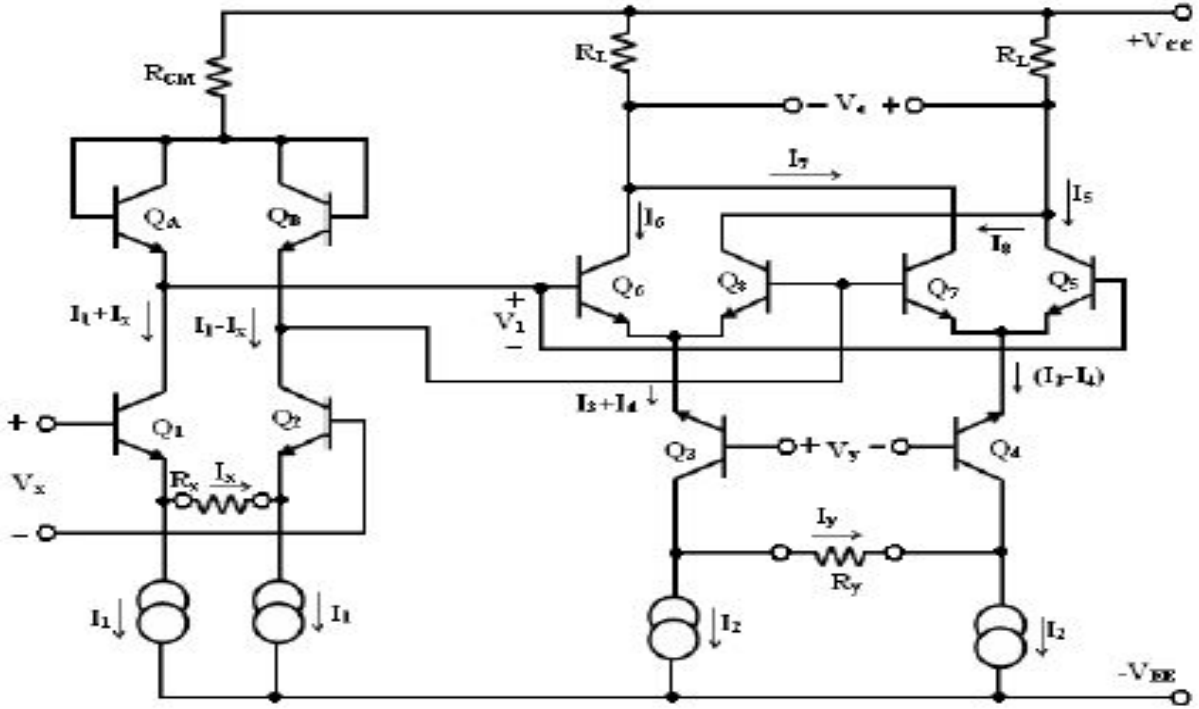
Variable Transconductance Technique:



$V0 = gm\ R_L Vx = (Vy/VTRE)VxRL$
$=(Vx\ Vy\ R_L/V_t\ R_e$

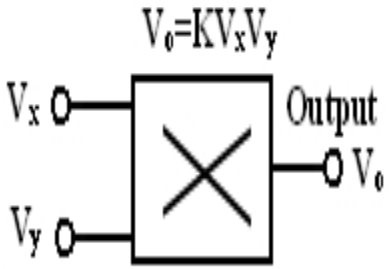
Four Quadrant Variable transconductance multiplier

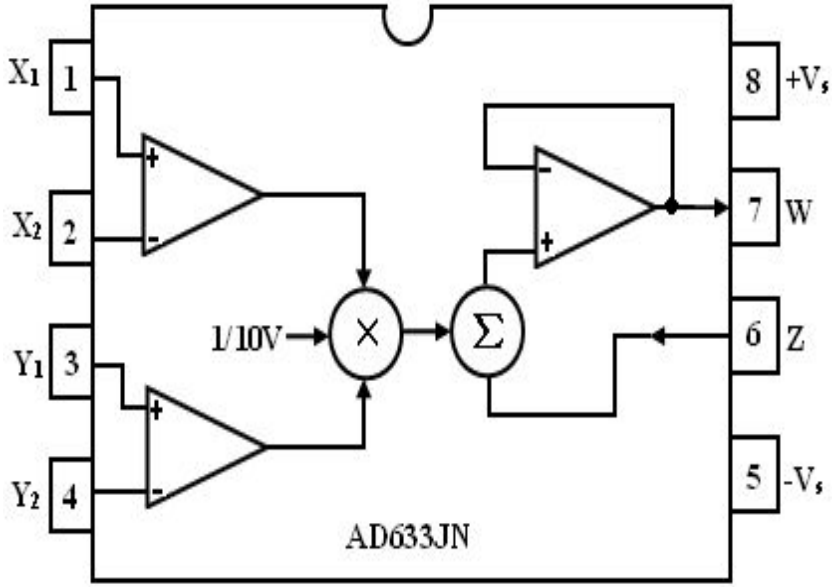
- The four quadrant operation indicates that the output voltage is directly proportional to the product of the two input voltages regardless of the polarity of the inputs and such multipliers can be operated in all the four quadrants of operation



Analog Multiplier ICs

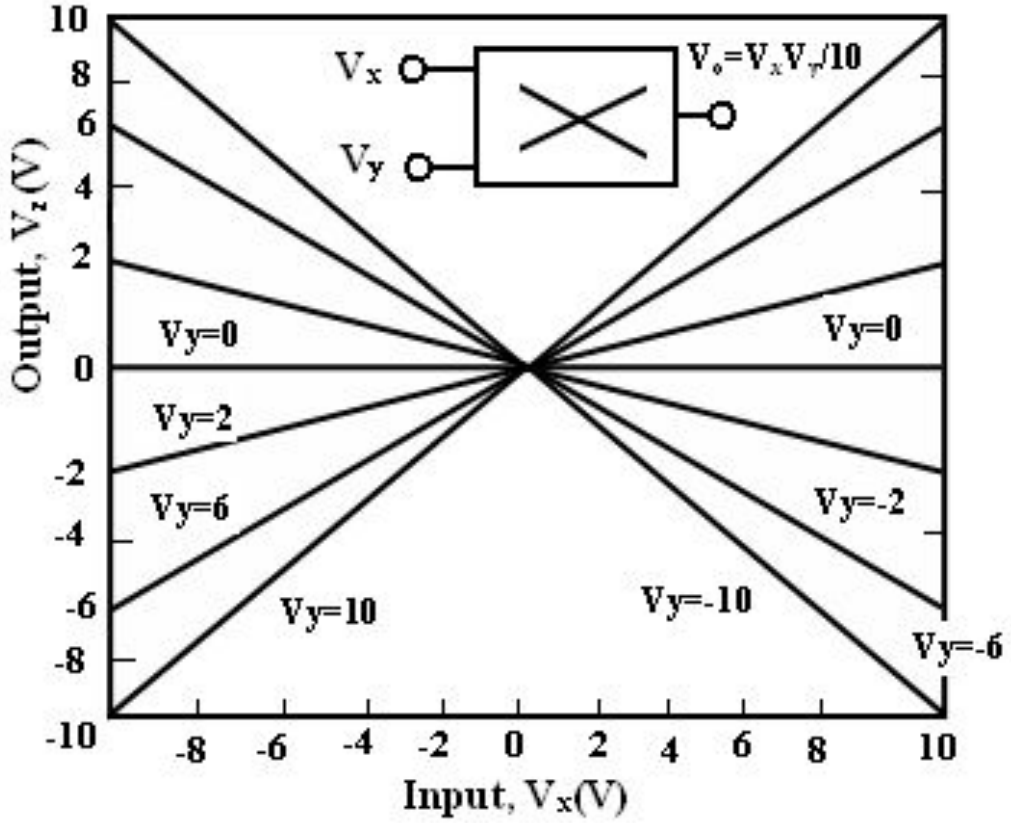
- Analog multiplier is a circuit whose output voltage at any instant is proportional to the product instantaneous value of two individual input voltages.
- The important applications----multiplication, division, squaring and square – rooting of signals, modulation and demodulation.
- These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. V0 =VxVy/10





Multiplier quadrants:

- The transfer characteristics of a typical four-quadrant multiplier is shown in figure. Both the inputs
  can be positive or negative to obtain the corresponding output as shown in the transfer
  characteristics.



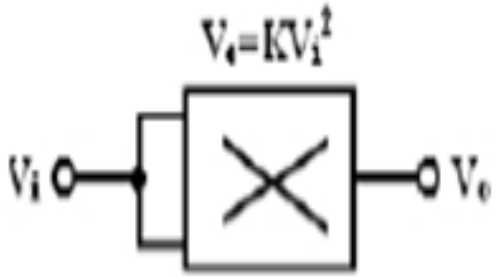
Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doubler
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

Voltage Squarer:

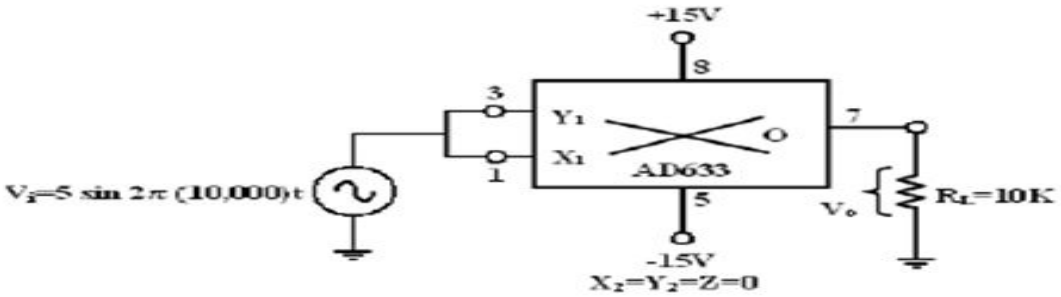
- Figure shows the multiplier IC connected as a squaring circuit. The inputs can be positive or
negative, represented by any corresponding voltage level between 0 and 10V.
- The input voltage Vi to be squared is simply connected to both the input terminals, and hence we have, Vx = Vy = Vi and the output is V0 = K Vi^2 .
- The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

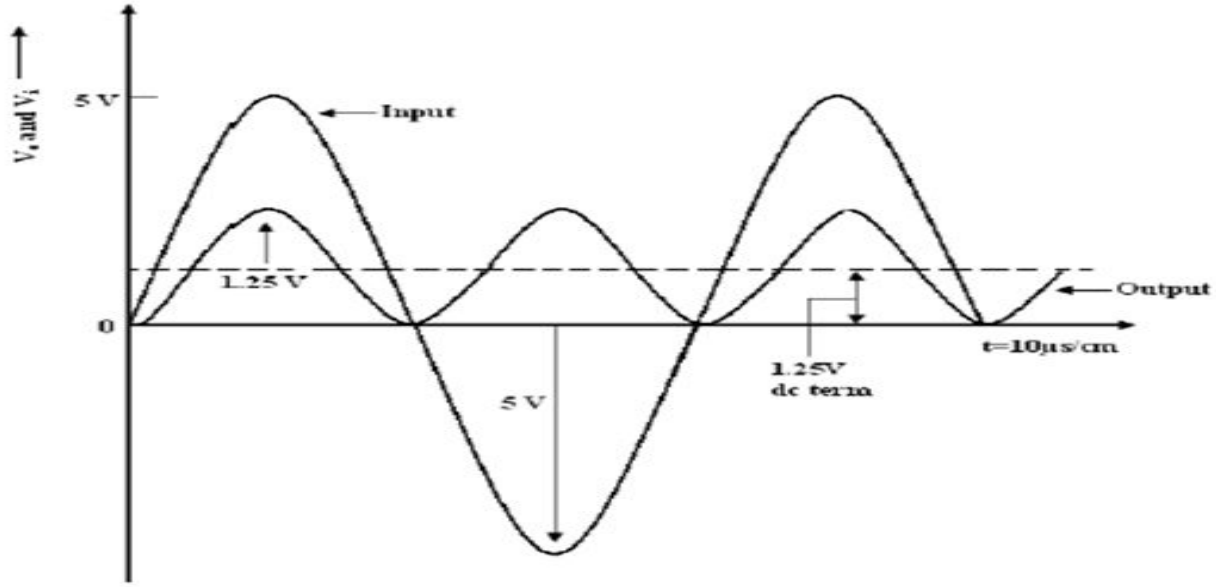


Frequency doubler

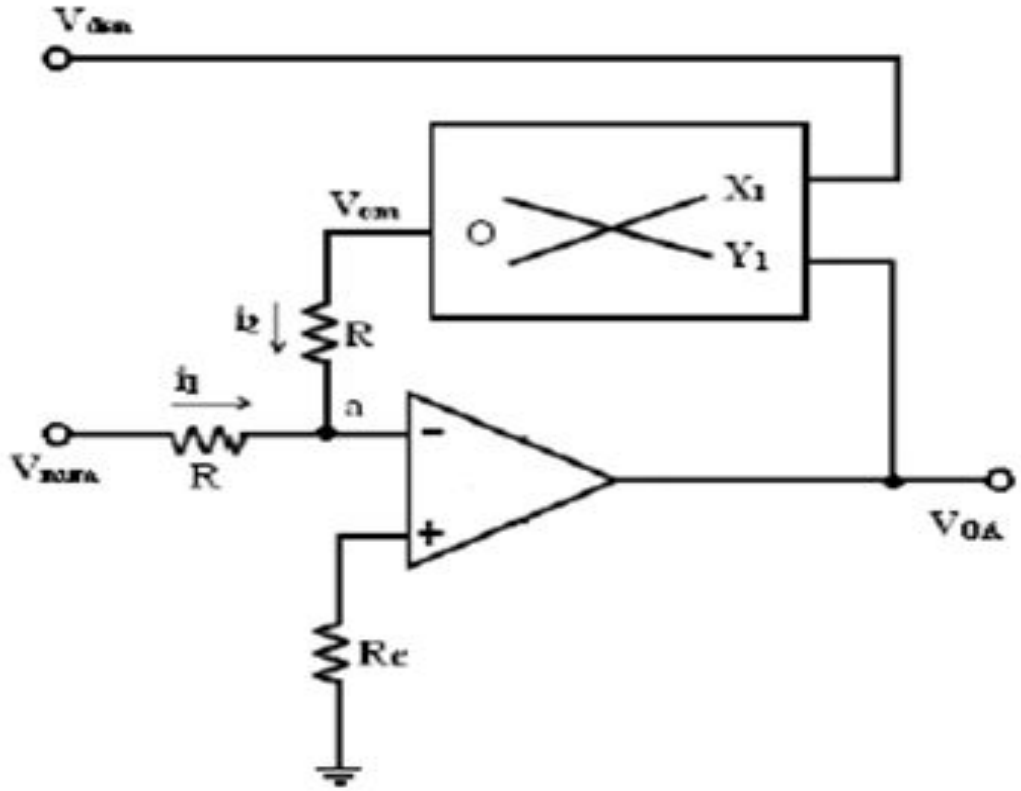
- A sine-wave signal Vi has a peak amplitude of Av and frequency of fHz.
- Assuming a peak amplitude Av of 5V and frequency f of 10KHz, V0 =1.25 – 1.25 cos2Π(20000)t.
  The first term represents the dc term of 1.25V peak amplitude .
- The output waveforms ripples with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals. The dc component of output V0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

Frequency doubler

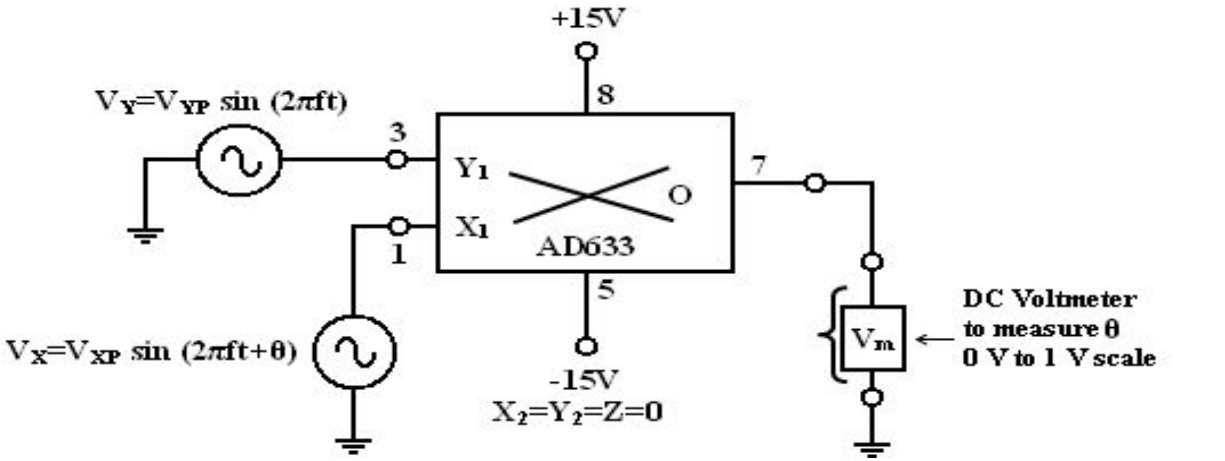


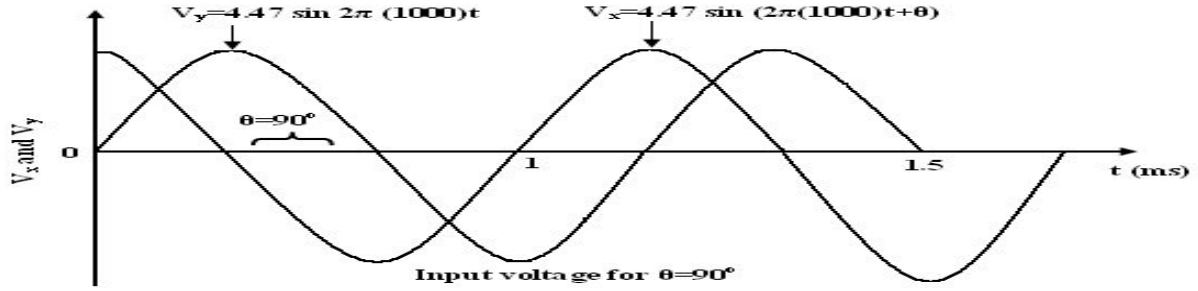


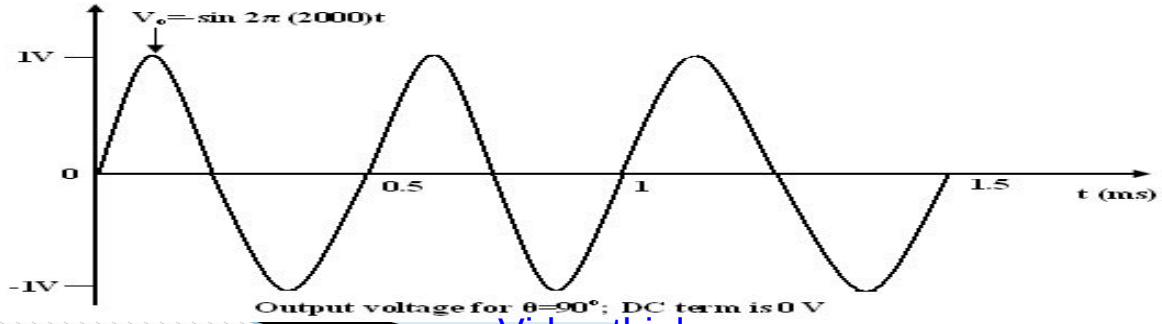
Voltage Divider



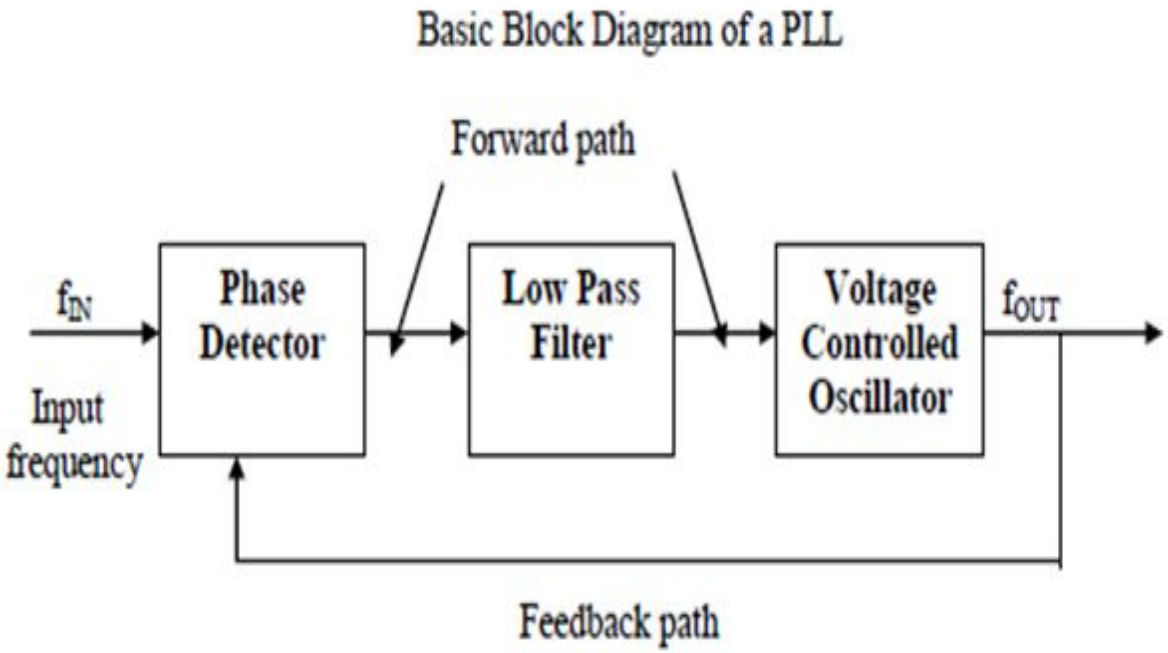
Phase angle Detector







PHASE LOCKED LOOP



PLL

Phase detector (PD):

- Analog multiplier
- PD produces an error signal that is proportional to the *phase error*, i.e., to the difference between the phases of input and output signals of the phase-locked loop

Loop filter:

- Low-pass filter
- It is characterized by its transfer function $F(s)$
- Low-pass filter suppresses the noise and unwanted PD outputs. It determines the *dynamics* of phase-locked loop

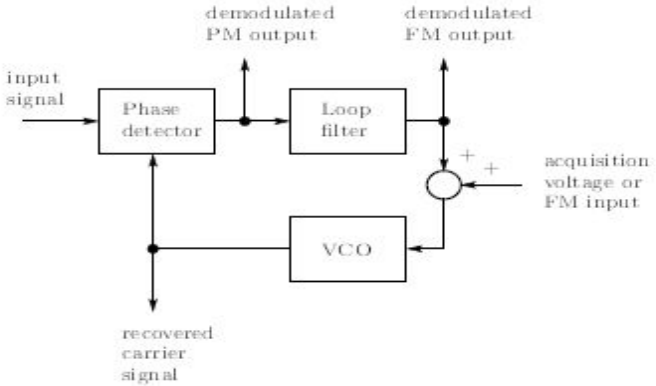
Voltage-controlled oscillator (VCO):

- VCO generates a sinusoidal signal
- The instantaneous VCO frequency is controlled by its input voltage

PLL

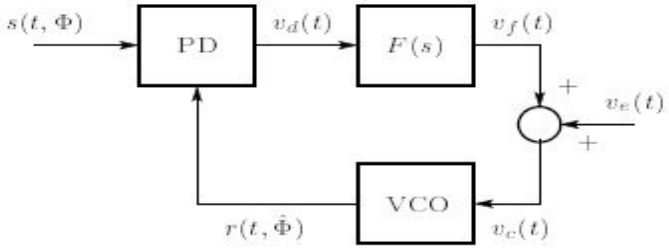
OPERATION PRINCIPLE OF PHASE-LOCKED LOOP – Part I

Basic loop configuration



PLL block diagram

Voltages appearing in the loop are also shown



Phase detector (PD) compares the phase of the input signal $s(t, \Phi)$ against the phase of the VCO output $r(t, \hat{\Phi})$ and produces an error signal $v_d(t)$

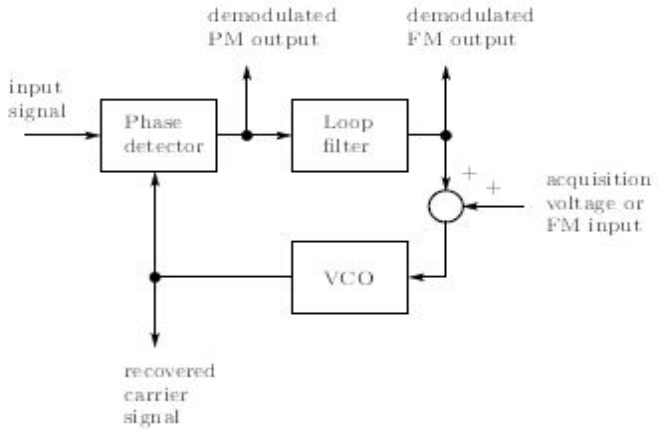
This error signal is then filtered, in order to remove noise and other unwanted components of the input spectrum

The sum of filter output $v_f(t)$ and an additive external control voltage $v_e(t)$ controls the instantaneous VCO frequency

PLL

OPERATION PRINCIPLE OF PHASE-LOCKED LOOP – Part II

Basic loop configuration



PLL block diagram

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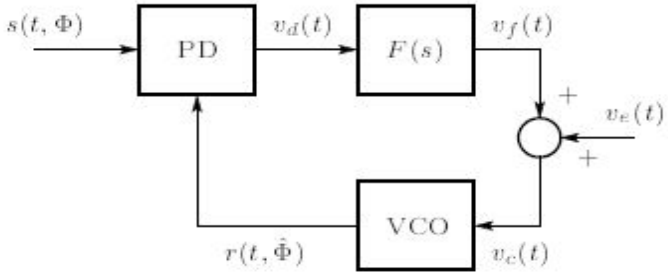


A nonzero output voltage must be provided by the PD, in order to tune the VCO frequency to the input one if the input frequency differs from the VCO center frequency

Consequently, the PLL tracks the phase of input signal with some phase error. However, this phase error can be kept very small in a well-designed PLL

PLL- construction and operation

➢
The phase detector or comparator compares the input frequency fs with feedback frequency fo. The output of the phase detector is proportional to the phase difference between fs & fo. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.

➢LPF removes the high frequency noise and produces a dc level. The high frequency component (fs + fo) is removed by the low pass filter

➢ The output frequency of VCO is directly proportional to the dc level. The VCO frequency is
compared with input frequency and adjusted until it is equal to the input frequencies.

➢ PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

➢Before the input is applied, the PLL is in free running state.

➢Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode.

➢ When Phase locked the loop tracks any change in the input frequency through its repetitive

PLL

➢The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs – fo) components at its output. The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO.

➢The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked.

➢ Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked,PLL tracks the frequency changes of the input signal.

➢ Thus, a PLL goes through three stages (i)free running, (ii) capture and (iii) locked or tracking.

➢Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

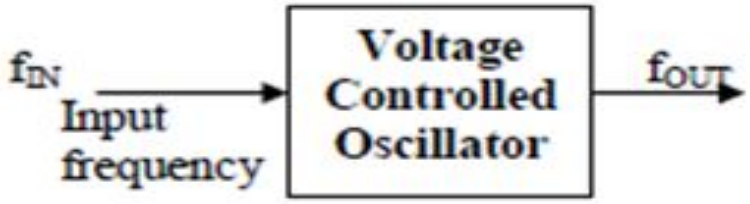
Low – Pass filter

- The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise.
- LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

  Lock range(Tracking range):The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.
- Capture range:Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.
- Filter Bandwidth:Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

Voltage Controlled Oscillator (VCO)

- The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage.
- **Voltage controlled oscillator**
- A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage
- The maximum output frequency of NE/SE 566 is 500 Khz.



Equations

$x_m(t)$ is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input $y(t)$ as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where g_v is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$x_f(t) = F_{\text{filter}}(x_m(t))$$

where F_{Filter} is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = x_f(t) = F_{\text{filter}}(x_m(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$x_c(t) = A_c \sin(\omega_c t).$$

The output of the phase detector then is:

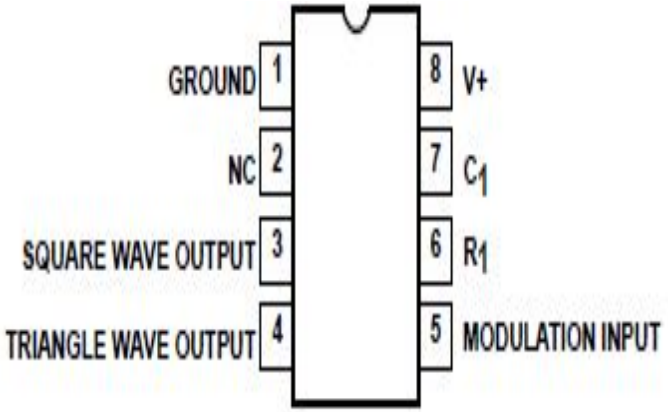
$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

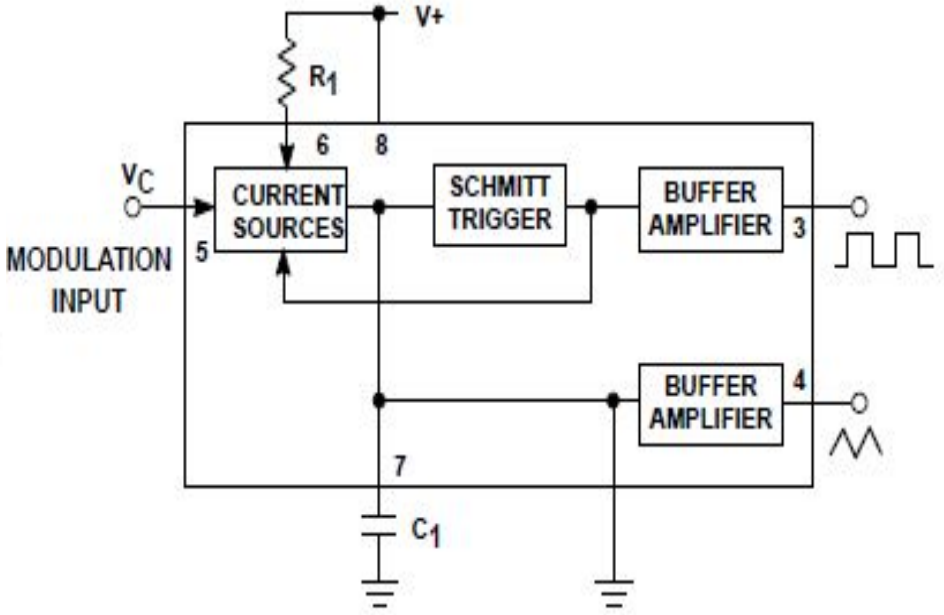
This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$ can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be *locked* if this is the case.

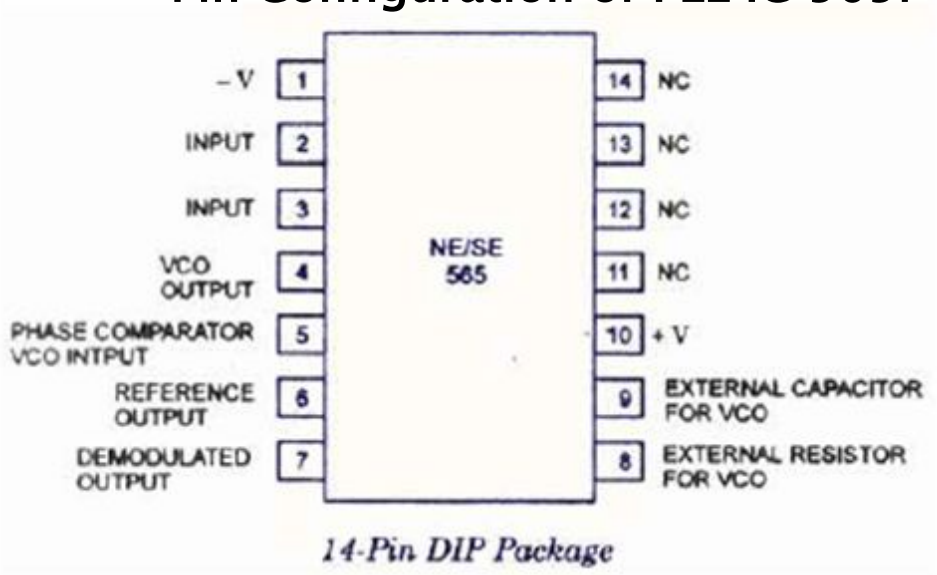
Monilithic VCO–IC 566





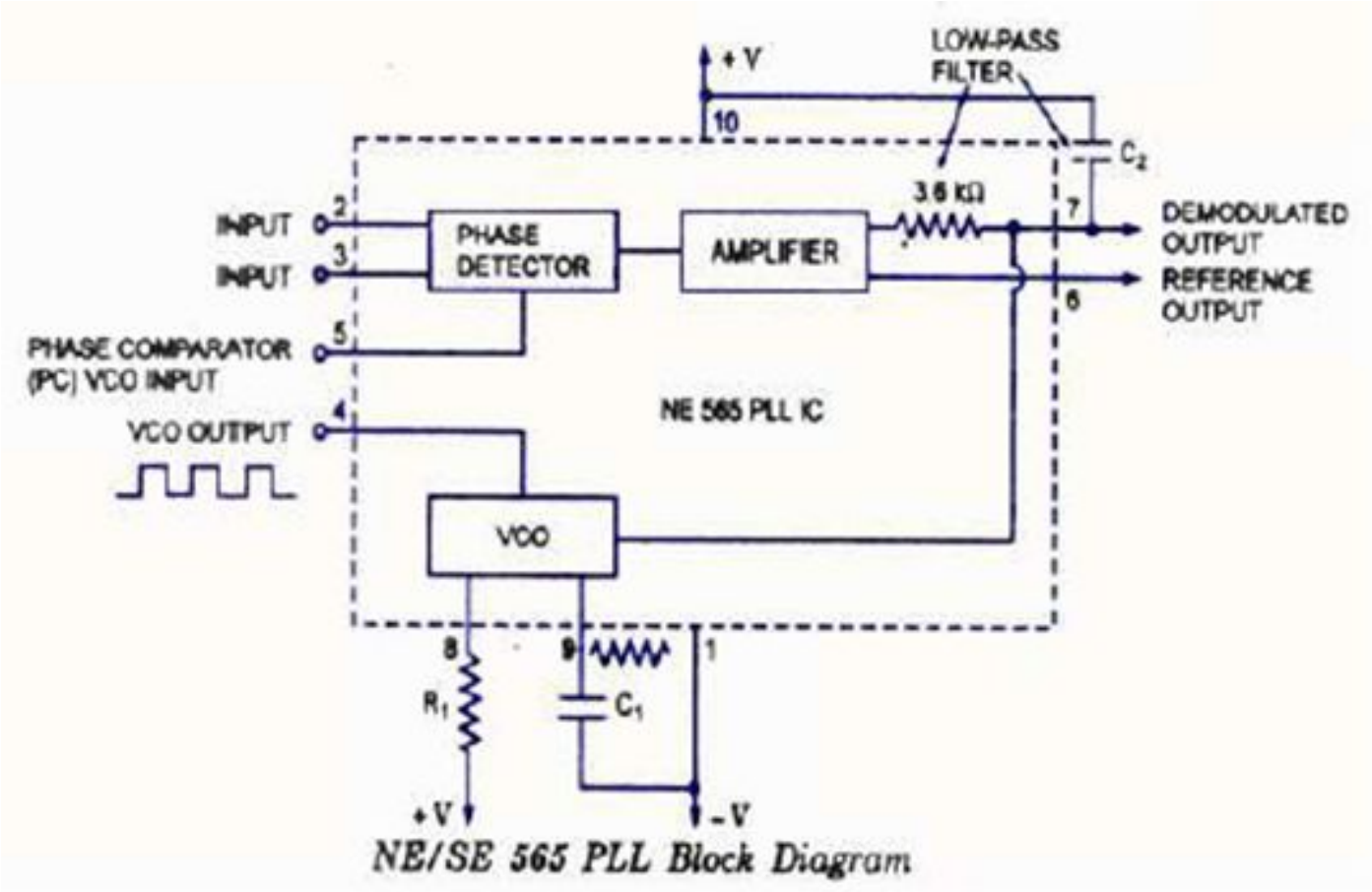
MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565)

Pin Configuration of PLL IC 565:



14-Pin DIP Package

Block Diagram



NE/SE 565 PLL Block Diagram

IC565

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561,
562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges.
The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz} \text{----------(1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

IC565

- The lock range fL & capture range fc of PLL is given by,

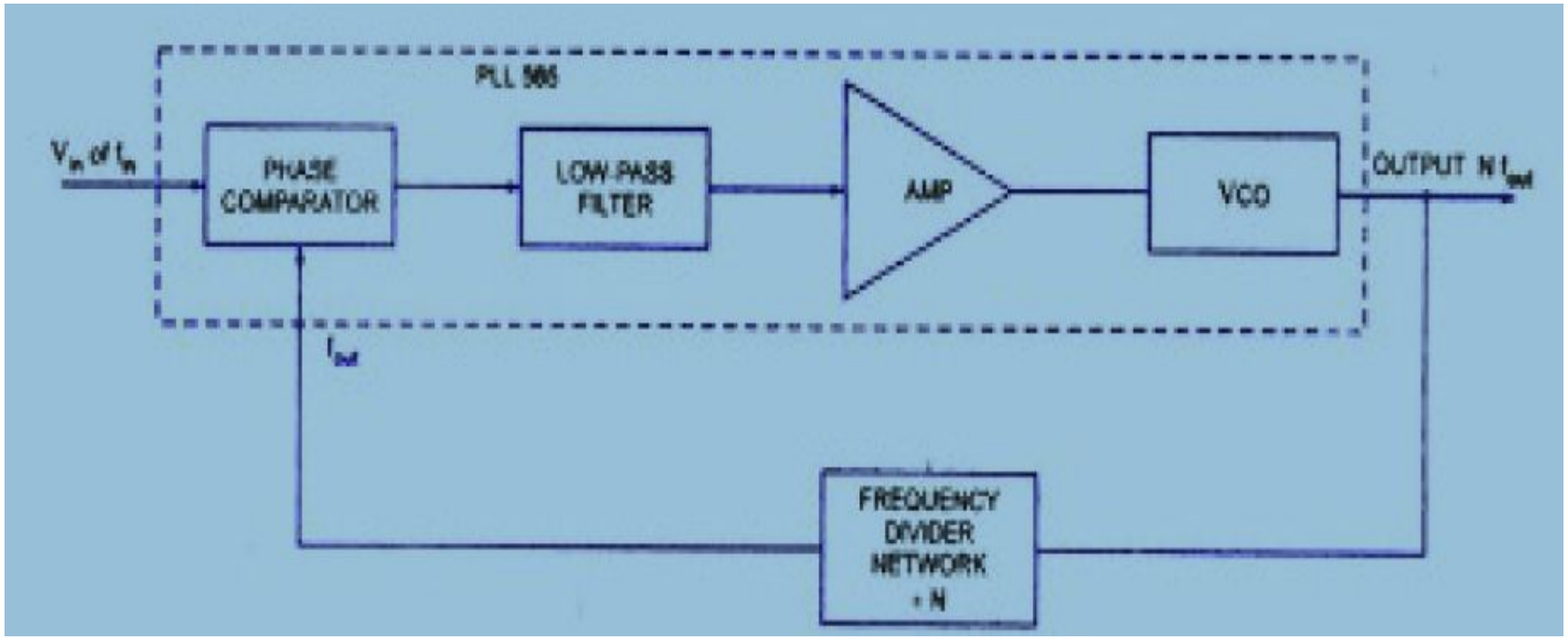
$$f_L = \pm \frac{8\ f_{out}}{V}\ Hz \quad \text{----------(2)}$$

Where f_{OUT} = free running frequency of VCO (Hz)

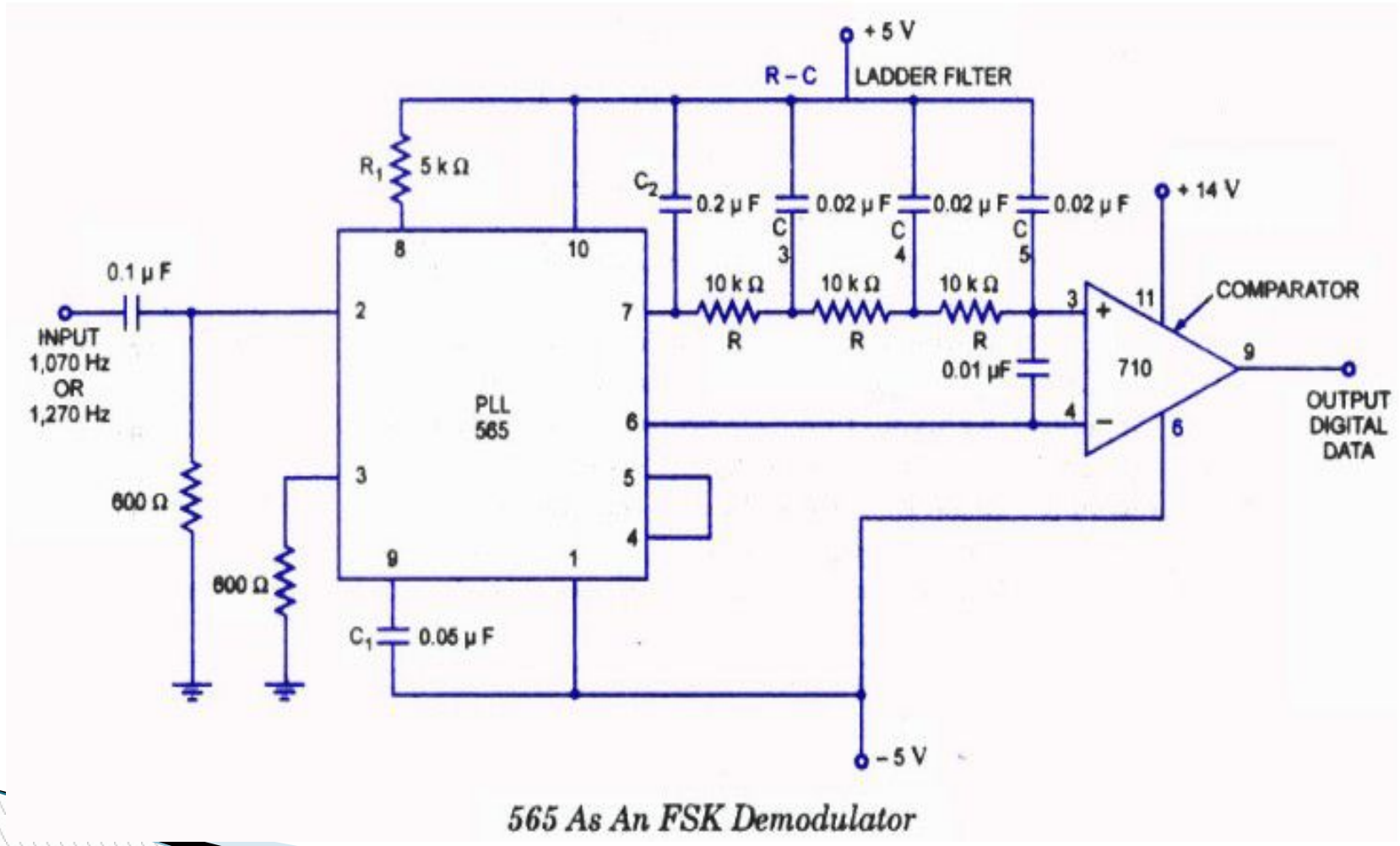
V = (+V)-(-V) volts

$$f_C = \pm \left[\frac{f_L}{(2\Pi)(3.6)(10^3)C_2} \right]^{1/2} \quad \text{----------(3)}$$

Applications of PLL-IC
1.Frequency Multiplier



2.FSK Demodulator



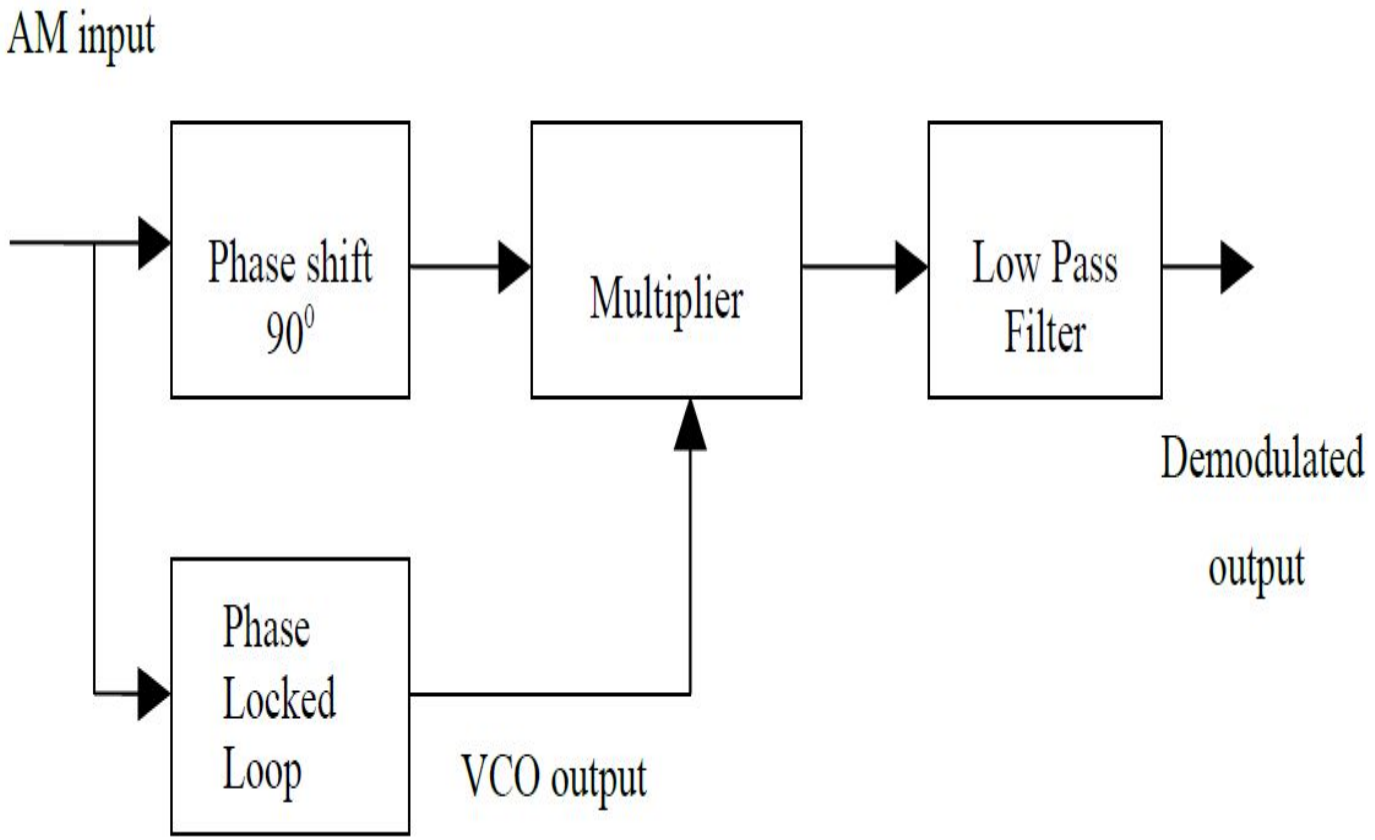
565 As An FSK Demodulator

FSK Demodulator

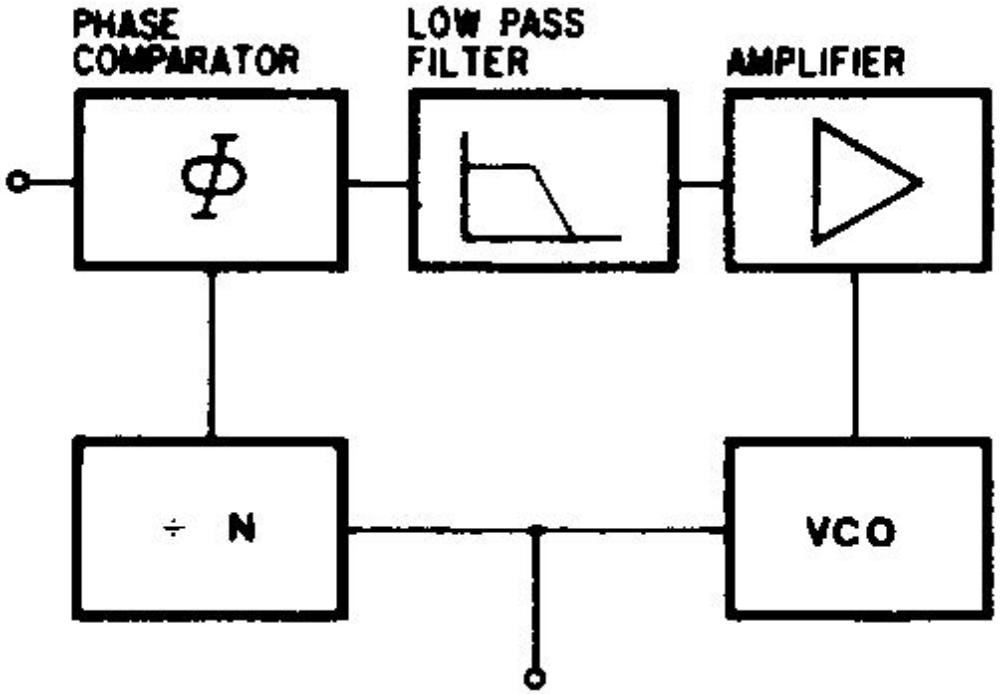
- · The output of 555 FSK generator is applied to the 565 FSK demodulator.
- · Capacitive coupling is used at the input to remove dc line.
- · At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- · R1 & C1 determine the free running frequency of the VCO, 3 stage RC ladder filter is used to

  remove the carrier component from the output.

3.AM Demodulation



4.Frequency multiplication/division:



5.Frequency Synthesizer