A

***Course File Report***

**On**

***“*COMPUTER ORGANISATION & ARCHITECTURE*”***

**Submitted by**

**Mr. B. KISHORE KUMAR Asst.Professor,**

*Department of*

CSE-DATA SCIENCE



***CMR ENGINEERING COLLEGE***

**(Affiliated to J.N.T.U, HYDERABAD)**

Kandlakoya(v),Medchal -501 401

**(2021-2022)**

**COURSE FILE**

**Subject: COMPUTER ORGANISATION & ARCHITECTURE**

 **Year: II– Year II SEM Branch: CSE-DATA SCIENCE**

|  |  |
| --- | --- |
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**1.Department vision & mission**

**Vision**

To create the next generation and globally competent data scientists/data engineers in the field of Data Science domain by providing quality engineering education along with cutting edge technologies

**Mission**

M1. To provide value based engineering education through continues learning and research by imparting solid foundation in applied mathematics, algorithms and programming paradigms to build software models and simulations.

M2. To develop concepts building, logical and problem solving skills of graduates to address current global challenges of industry and society.

M3. To offer excellence in teaching and learning process, industry collaboration activities and research to mould graduates into industry ready professionals

**2.1 Program Educational outcome (PEO):**

* Excel in professional career or higher education by acquiring knowledge in mathematical, computing and engineering principles
* To provide intellectual environment for analyzing and designing computing systems for technical needs
* Exhibit professionalism, multidisciplinary teamwork and adapt to current trends by engaging in lifelong learning and practice their profession with legal, social and ethical responsibilities

**2.2 Program Outcome (PO):**

1. **Engineering knowledge:** An ability to apply knowledge of computing, mathematics, science and engineering fundamentals appropriate to the discipline
2. **Problem analysis:** An ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution
3. **Design/development of solutions:** An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs with appropriate consideration for public health and safety, cultural, societal and environmental considerations
4. **Conduct investigations of complex problems:** An ability to design and conduct experiments, as well as to analyze and interpret data
5. **Modern tool usage:** An ability to use current techniques, skills, and modern tools necessary for computing practice
6. **The engineer and society:** An ability to analyze the local and global impact of computing on individuals, organizations, and society
7. **Environment and sustainability:** Knowledge of contemporary issues
8. **Ethics:** An understanding of professional, ethical, legal, security and social issues and responsibilities
9. **Individual and team work:** An ability to function effectively individually and on teams, including diverse and multidisciplinary, to accomplish a common goal
10. **Communication:** An ability to communicate effectively with a range of audiences
11. **Project management and finance:** An understanding of engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects
12. **Life-long learning:** Recognition of the need for and an ability to engage in continuing professional development

**PROGRAM SPECIFIC OUTCOMES (PSO’S)**

1. **Professional Skills and Foundations of Software development:** Ability to analyze, design and develop

applications by adopting the dynamic nature of Software developments

2. **Applications of Computing and Research Ability:** Ability to use knowledge in cutting edge technologies in identifying research gaps and to render solutions with innovative ideas

**3. List of cos(Action verbs as per Bloom's Taxonomy)**

|  |  |
| --- | --- |
| **CO1** | **Define** the basic components of a digital computer |
| CO2 | **Design** of CPU, ALU and Control Unit |
| CO3 |  |
| CO4 | **Analyze** Input output organization |
| CO5 | **Determine** the memory hierarchy, parallelism and pipelining for high performance processor |

**4. Syllabus Copy and Suggested/Reference Books**

**UNIT – I**

**Digital Computers:** Introduction, Block diagram of Digital Computer, Definition of Computer

Organization, Computer Design and Computer Architecture.

**Register Transfer Language and Micro operations:** Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

**Basic Computer Organization and Design:** Instruction codes, Computer Registers Computer

Instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

**UNIT – II**

**Micro programmed Control:** Control memory, Address sequencing, micro program example, design of control unit.

**Central Processing Unit:** General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

**UNIT – III**

**Data Representation:** Data types, Complements, Fixed Point Representation, Floating Point

Representation.

**Computer Arithmetic:** Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

**UNIT – IV**

**Input-Output Organization:** Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

**Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

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**UNIT – V**

**Reduced Instruction Set Computer:** CISC Characteristics, RISC Characteristics.

**Pipeline and Vector Processing:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction

Pipeline, RISC Pipeline, Vector Processing, Array Processor.

**Multi Processors:** Characteristics of Multiprocessors, Interconnection Structures, Interprocessor

arbitration, Interprocessor communication and synchronization, Cache Coherence.

**TEXT BOOK:**

 1. **Computer System Architecture** – M. Moris Mano, Third Edition, Pearson/PHI.

**REFERENCES:**

1. **Computer Organization** – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw

Hill.

2. **Computer Organization and Architecture** – William Stallings Sixth Edition, Pearson/PHI.

3. **Structured Computer Organization** – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

5. Session Plan/Lesson Plan

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No** | **Topic(JNTU syllabus)** | **Sub-Topic** | **No. Of Lectures Required** | **Suggested Books** | **Remarks** |
| 1 | **UNIT-I****Digital Computer, Register Transfer Language And Microoperations,Basic Computer Organization And Design** | Introduction, Block diagram of Digital Computer | L1 | T1 |  |
| 2 | Definition ofComputer Organization, Computer Design and Computer Architecture. | L2 | T1 |  |
| 3 | Instruction codes | L3 | T1 |  |
| 4 | Computer Registers | L4 | T1 |  |
| 5 | Computer instructions | L5 | T1 |  |
| 6 | Timing and Control | L6 | T1 |  |
| 7 | Instruction cycle | L7 | T1 |  |
| 8 | Memory Reference Instructions | L8 | T1 |  |
| 9 | Input – Output and Interrupt | L9 | T1 |  |
| 10 | Complete Computer Description | L10 | T1 |  |
|  |  | **Total required** | **10** |  |  |
| 11 | **UNIT - II****Micro Programmed Control, CPU** | Control memory | L11 | T2 |  |
| 12 | Address sequencing | L12 | T2 |  |
| 13 | micro program example | L13 | T2 |  |
| 14 | General Register Organization | L14 | T2 |  |
| 15 | Instruction Formats | L15 | T2 |  |
| 16 | Addressing modes | L16 | T2 |  |
| 17 | Data Transfer and Manipulation | L17 | T2 |  |
|  | Program Control. | L18 | T2 |  |
| 18 | design of control unit | L19 | T2 |  |
|  |  | **Total Required** | **9** |  |  |
| 19 | **UNIT – III****Data Representation, Computer Arithmetic** | Data Types | L20 | T2 |  |
| 20 | Complements | L21 | T2 |  |
| 21 | Fixed Point Representation | L22 | T2 |  |
| 22 | Floating PointRepresentation. | L23 | T2 |  |
| 23 | Addition And Subtraction | L24 | T2 |  |
| 24 | Multiplication Algorithms | L25 | T2 |  |
| 25 | Division Algorithms | L26 | T2 |  |
| 26 | Floating – Point Arithmetic Operations. | L27 | T2 |  |
| 27 | Decimal Arithmetic Unit | L28 | T2 |  |
| 28 | Decimal Arithmetic Operations. | L29 | T2 |  |
|  |  | **Total Required** | **10** |  |  |
| 30 | **UNIT-IV****I/O Organization, Memory Organization** | Peripheral Devices | L30 | T1 |  |
| 31 | Input-Output Interface | L31 | T1 |  |
| 32 | Asynchronous Data Transfer | L32 | T1 |  |
| 33 | Modes Of Transfer | L33 | T1 |  |
| 34 | Priority Interrupt | L34 | T1 |  |
| 35 | Direct Memory Access | L35 | T1 |  |
| 36 | Input –Output Processor (Iop) | L36 | T1 |  |
| 37 | Memory Hierarchy | L37 | T1 |  |
| 38 | Main Memory | L38 | T1 |  |
| 39 | Auxiliary Memory | L39 | T1 |  |
| 40 | Associate Memory | L40 | T1 |  |
| 41 | Cache Memory | L41 | T1 |  |
|  |  | **Total Required** | **12** |  |  |
| 42 | **UNIT-V****RISC, Pipeline And Vector Processing ,****Multiprocessor** |  |  |  |  |
| 42 | CISC AND RISC | L42 | T1 |  |
| 43 | Parallel Processing | L43 | T1 |  |
| 44 | Pipelining, Arithmetic Pipeline | L44 | T1 |  |
| 45 | Instruction Pipeline | L45 | T1 |  |
| 46 | Risc Pipeline | L46 | T1 |  |
| 47 | Vector Processing, | L47 | T1 |  |
| 48 | Characteristics Of Multiprocessors | L48 | T1 |  |
| 49 | Interconnection Structures | L49 | T1 |  |
| 50 | Interprocessor Arbitration | L50 | T1 |  |
| 51 | Array Processors | L51 | T1 |  |
| 52 | Inter Processor Communication, And Synchronization | L52 | T1 |  |
|  |  | **Total Required** | **11** |  |  |

1. **Session execution log**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S no** | **Unit** | **Scheduled completed date** | **Completed date** | **Remarks** |
| **1** | **I** | **10/03/2022** | **12/03/2022** |  |
| **2** | **II** | **23/03/2022** | **29/03/2022** |  |
| **3** | **III** | **25/04/2022** | **05/05/2022** |  |
| **4** | **IV** | **15/05/2022** | **23/05/2022** |  |
| **5** | **V** | **01/06/2022** | **02/06/2022** |  |

**7.Lecture Notes**

**8.Assignment Questions along with sample Assignments Scripts**

**ASSIGNMENT QUESTIONS**

**MID-I**

**1. Explain about block diagram of digital computer? (CO1)**

**2. What do understand by Instruction cycle? Draw and explain the flowchart for an instruction to execute (CO1)**

**3. Explain different types of Addressing Modes with example? (CO2)**

**4. Explain different types of Micro Operations? (CO2)**

**5. Write about different types of number systems (CO3)**

**MID-II**

**1. Write About booth Multiplication Algorithm? (CO3)**

**2. Explain About DMA controller? (CO4)**

**3. Explain cache memory? (CO4)**

**4. Deference between RISC AND CISC? (CO5)**

**5. Explain the difference between vector processing and array processing? (CO5)**

**9.Mid exam Question Papers along with sample Answers Scripts**

**MID-I QUESTION PAPER**

**Subject Computer Organization&Architecture Branch CSE\_DATA SCIENCE**

Answer The Following Questions Max Marks 25

 PART-A

1.What is meant by system bus?

2.define computer organization and architecture?

3.List out different registers part of a main memory&control memory

4.explain the difference between hardwired and micro program control

5.what are the different types of number systems

 PART\_B

6.Draw the hardware architecture of 4-bit binary addersubtracter

 (OR)

7.with a suitable figure explain the architecture of van Neumann architecture?

8.wgat is instruction cycle?explain with the help of a diagram?

(OR)

9.describe the micro programmed control organization and compare cons and pros

10.convert the following number systems

 A)(1259)10 to hexadecimal andbinary,octal

 B)(1001001110101101)2 to hexadecimal,decimal

(OR)

11.find the r’s (r-1)’s complement A)(10101)2 B)9753)10

**MID-II QUESTION PAPER**

**Subject Computer Organization&Architecture Branch CSE\_DATA SCIENCE**

Answer The Following Questions Max Marks 25

 PART-A **5\*2=10**

1.Explain I/O interface?( CO4)

2.Discuss about Auxiliary memory

3.Define pipeline? and explain pipeline types?( CO5)

4.Write about memory Hierarchy?(CO4)

5.Characteristics of Multiprocessor?(CO5)

 PART\_B **3\*5=15**

6.Explain multiplication algorithm? With example?( CO3)

 (OR)

7.Explain Booth Algorithm ?(CO3)

8. Explain about a) DMA b) ADT (CO4)

(OR)

9. Discuss a) Cache Memory b) Associate Memory (CO4)

10.Explain CISC and RISC?(CO5)

 (OR)

11 Explain Vector Processing? And Cache Coherence?(CO5)

**10. Scheme of Evaluation**

**Branch: CSE-DATA SCIENCE Year: II-II Total marks: 25**

 **MD I**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **THEORY** | **MARKS** | **TOTAL** |
| **PART-A** |
| 1 | Diagram of system bus | 2 | 2 |
| 2 | Definition of coDefinition of ca | 11 | 2 |
| 3 | Typesofregistersexplanation | 11 | 2 |
| 4 | table | 2 | 2 |
| 5 | TypesExample | 11 | 2 |
| **PART-B** |
| 6 | Diagramexplanation | 2.52.5 | 5 |
| 7 | Diagramexplanation | 2.52.5 | 5 |
| 8 | Instruction cycle stagesdiagram | 2.52.5 | 5 |
| 9 | ExplanationPros and cons | 2.52.5 | 5 |
| 10 | A)Decimal to binaryDecimal to hexadecimalDecimal to octalB)binary to decimalBinary to hexadecimal | 11111 | 5 |
| 11 | 1’scomplement,9’s complement2’s complement10’s complement | 11.511.5 | 5 |

 **MID II**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No.** | **THEORY** | **MARKS** | **TOTAL** |
| **PART-A** |
| 1 | Diagram of interfaceNeed&explanation | 11 | 2 |
| 2 | Definition example | 11 | 2 |
| 3 | DefinitionTypes | 11 | 2 |
| 4 | List of memoryComparision of memory | 11 | 2 |
| 5 | charecterstics | 2 | 2 |
| **PART-B** |
| 6 | Flowchart&processexample | 32 | 5 |
| 7 | Flowchart&processexample | 32 | 5 |
| 8 | DiagramExplanationTypesexplanation | 11.511.5 | 5 |
| 9 | Mapping typesExplanationDiagramexplanation | 11.511.5 | 5 |
| 10 | Risc diagramCharactersticsCisc diagramcharacterstics | 11.511.5 | 5 |
| 11 | ExplanationProblemsolution | 2.511.5 | 5 |

**11.Mapping of COs with POs and PSOs**

**1 – Slightly 2 – Moderately 3 – Substantive**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Outcomes (CO)** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO 1** | **PSO 2** |
| 1 | 1 | - | 1 | - | - | - | - | - | - | - | - | - | 1 | - |
| 2 | 1 | 1 | 3 | 1 | 2 | - | - | - | - | - | - | 1 | - | 1 |
| 3 | - | - | 1 | 1 | 1 | - | - | - | - | - | - | - | - | - |
| 4 | 1 | 3 | 2 | 2 | 2 | 1 | - | - | - | - | - | 1 | - | 2 |
| 5 | 1 | 1 | 2 | 3 | 1 | - | - | - | - | - | - | - | 2 | - |
| 6 | 1 | 1 | 2 | 1 | 3 | 1 | 1 | - | - | - | - | - | - | - |
|   | **1** | **1** | **2** | **1** | **0** | **-** | **-** | **-** | **-** | **-** | **-** | **0** |  |  |

**12.Attainment of Cos,POs and PSOs (Excel Sheet)**

**13.UniversityQuestionPapers/QuestionBank**

**CodeNo:153AG R18**

**JAWAHARLALNEHRUTECHNOLOGICALUNIVERSITYHYDERABAD**

**B.TechIIYearISemester Examinations,October2020**

**COMPUTERORGANIZATIONANDARCHITECTURE**

 **(ComputerScienceandEngineering)**

**Time:2hours Max.Marks:75**

**Answer anyfivequestionsAllquestionscarryequalmarks---**

**1.a)Drawthebus systemforfour registersandexplain.**

**b)An8bitregistercontainsthebinaryvalue10011100.WhatistheregistervalueafteranArithmeticShiftRight?Startingfromthe initialnumber10011100,determine the registervalueafteran arithmetic ShiftLeft,andstatewhetherthereisanoverflow. [7+8]**

**2.Drawblockdiagramofacontrolmemoryandtheassociatedhardwareneededforselectingthenextmicroinstructionaddress. [15]**

**3.Performthearithmeticoperation(+42)+(-13)and(-42)-(13)inbinaryusingsigned2’scomplementrepresentationfornegativenumbers. [15]**

**4.a)DifferentiatebetweenIsolated I/Oandmemory-mapped I/O.**

**b)Explainprogrammed-I/O indetail. [8+7]**

**5.a)WritethemajorcharacteristicsofRISCprocessors.**

**b)Drawaspace-timediagramforafour-segmentpipelineshowingthetimeittakestoprocesssixtasksandexplain. [7+8]**

**6.a)Drawthe flowchartforinstructioncycleandexplain.**

**b)Explainthefollowinginstructions:BUN,ISZ, BSA,LDA,STA. [7+8]**

**7.ExplainvariousData Manipulationinstructionswith examples. [15]**

**8.Withanexample,explainBoothMultiplicationalgorithm. [15]**

**13**

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**14.Power point presentations (PPTs)**

|  |  |  |
| --- | --- | --- |
| Unit no  | Topic name  | Link |
| 1 | Instruction code | https://www.youtube.com/watch?v=mEw09EJwj30 |
| 1 | Instruction cycle | https://www.youtube.com/watch?v=SFsnysyVhzA |
| 1 | Microprogrammed control unit | <https://www.youtube.com/watch?v=81v7JqLbTMI>http://www.infocobuild.com/education/audio-video-courses/computer-science/ComputerOrganization-IIT-Madras/lecture-07.html |
| 2 | Architecture of 8086 | https://www.youtube.com/watch?v=CEL-jT4qFCk |
| 2 | Addressing modes of 8086 | https://www.youtube.com/watch?v=hVRtfcvt1ns |
| 2 | Instruction set of 8086 | https://www.youtube.com/watch?v=V3AeSmlZzw8 |
| 3 | Interrupts of 8086 | https://www.youtube.com/watch?v=LUVJxy-pGlM |
| 3 | Procedures and macros | https://www.youtube.com/watch?v=ybz0MYyum5M |
| 3 | Stack structure of 8086 | https://www.youtube.com/watch?v=t35b-8w4Yrg |
| 4 | Computer arthimatic(addition , substraction) | https://www.youtube.com/watch?v=o-WXqnagg0c |
| 4 | Floating point arthimatic(addition) | https://www.youtube.com/watch?v=KiWz-mGFqHI |
| 4 | Asynchronous data transfer | https://www.youtube.com/watch?v=EzEqUH93C4U |
| 5 | Memory organization | https://www.youtube.com/watch?v=z\_dSASDYc6c |
| 5 | Pipelining  | https://www.youtube.com/watch?v=hGjX1Iw9Qxw |
| 5 | Multiprocessors | https://www.youtube.com/watch?v=fG3pmE2iRzo |

**15.Websites/URLs/ e- Resources**

• www.wiley.com

• www.faadooengineers.com

• www.scribd.com

• www.slideshare.net

• www.google.com/co

• www.bookadda.com

• <http://www.infocobuild.com>

• <http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT-%20Guwahati/comp_org_arc/web/>