# Unit # 5

**Pipeline and Vector Processing**

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**Characteristics of multiprocessors**

* A multiprocessor system is an interconnection of two or more CPUs with memory and input-output equipment.
* The term “processor” in multiprocessor can mean either a central processing unit (CPU) or an input-output processor (IOP).
* Multiprocessors are classified as multiple instruction stream, multiple data stream (MIMD) systems
* The similarity and distinction between multiprocessor and multicomputer are:

##### Similarity

* + - Both support concurrent operations
	+ **Distinction**
		- The network consists of several autonomous computers that may or may not communicate with each other.
		- A multiprocessor system is controlled by one operating system that provides interaction between processors and all the components of the system cooperate in the solution of a problem.

**Characteristics of multiprocessors**

* Multiprocessing improves the reliability of the system.
* The benefit derived from a multiprocessor organization is an improved system performance.
	+ Multiple independent jobs can be made to operate in parallel.
	+ A single job can be partitioned into multiple parallel tasks.
* Multiprocessing can improve performance by decomposing a program into parallel executable tasks.
	+ The user can explicitly declare that certain tasks of the program be

executed in parallel.

* + - This must be done prior to loading the program by specifying the parallel executable segments.
	+ The other is to provide a compiler with multiprocessor software that

can automatically detect parallelism in a user’s program.

## Characteristics of multiprocessors

* Multiprocessor are classified by the way their memory is organized.
	+ A multiprocessor system with common shared memory is classified as a shared-memory or tightly coupled multiprocessor.
		- Tolerate a higher degree of interaction between tasks.
	+ Each processor element with its own private local memory is classified as a distributed-memory or loosely coupled system.
		- Are most efficient when the interaction between tasks is minimal

### Interconnection Structures

* The components that form a multiprocessor system are CPUs, IOPs connected to input-output devices, and a memory unit.
* The interconnection between the components can have different physical configurations, depending on the number of transfer paths that are available
	+ Between the processors and memory in a shared memory system
	+ Among the processing elements in a loosely coupled system
* There are several physical forms available for establishing an interconnection network.
	+ Time-shared common bus
	+ Multiport memory
	+ Crossbar switch
	+ Multistage switching network
	+ Hypercube system

**Time Shared Common Bus**

* A common-bus multiprocessor system consists of a number of processors connected through a common path to a memory unit.
* Disadvantage.:
	+ Only one processor can communicate with the memory or another processor at any given time.
	+ As a consequence, the total overall transfer rate within the system is limited by the speed of the single path
* A more economical implementation of a dual bus structure is depicted in Fig. 5.1 and Fig. 5.2.
* Part of the local memory may be designed as a cache memory attached to the CPU.

# Time Shared Common Bus



**Figure 5.1: Time shared common bus organization**

## Time Shared Common Bus



**Figure 5.2: System bus structure for multiprocessors**

### Multiport Memory

* A multiport memory system employs separate buses between each memory module and each CPU.
* The module must have internal control logic to determine which port will have access to memory at any given time.
* Memory access conflicts are resolved by assigning fixed priorities to each memory port.
* *Advantage*:
	+ The high transfer rate can be achieved because of the multiple paths.
* *Disadvantage*:
	+ It requires expensive memory control logic and a large number of

cables and connections

* Fig. 5.3 shows multiport memory system.

## Multiport Memory



**Figure 5.3: Multiport memory organization**

### Crossbar Switch

* This consists of a number of *crosspoints* that are placed at intersections between processor buses and memory module paths.
* The small square in each crosspoint is a *switch* that determines

the path from a processor to a memory module.

##### Advantage:

* + Supports simultaneous transfers from all memory modules

##### Disadvantage:

* + The hardware required to implement the switch can become quite large and complex.
* Fig. 5.4 shows the functional design of a crossbar switch

connected to one memory module.

* Figure 5.5 shows Block diagram of crossbar switch.

## Crossbar Switch



**Figure 5.4: Crossbar switch**

## Crossbar Switch



**Figure 5.5: Block diagram of crossbar switch**

#### Multistage Switching Network

* The basic component of a multistage network is a two-input, two- output interchange switch as shown in below Figure.



## Multistage Switching Network

* + Using the 2x2 switch as a building block, it is possible to build a multistage network to control the communication between a number of sources and destinations.
		- To see how this is done, consider the binary tree shown in below Figure.
		- Certain request patterns cannot be satisfied simultaneously. i.e., if P1 - 000~011, then P2 - 100~111

## Multistage Switching Network

* One such topology is the omega switching network shown in Fig. 5.6.



**Fig. 5.6: 8 x 8 Omega Switching Network**

## Multistage Switching Network

* Some request patterns cannot be connected simultaneously. i.e., any two sources cannot be connected simultaneously to destination 000 and 001
* In a tightly coupled multiprocessor system, the source is a processor and the destination is a memory module.
* Set up the path transfer the address into memory transfer the data

**Hypercube System**

* + The hypercube or binary n-cube multiprocessor structure is a loosely coupled system composed of N=2n processors interconnected in an n-dimensional binary cube.
		- Each processor forms a node of the cube, in effect it contains not only a CPU but also local memory and I/O interface.
		- Each processor address differs from that of each of its n neighbors by exactly one bit position.
	+ Fig. 5.7 shows the hypercube structure for n=1, 2, and 3.
	+ Routing messages through an *n*-cube structure may take from one to *n* links from a source node to a destination node.
		- A routing procedure can be developed by computing the exclusive-OR of

the source node address with the destination node address.

* + - The message is then sent along any one of the axes that the resulting binary value will have 1 bits corresponding to the axes on which the two nodes differ.

## Multistage Switching Network

* A representative of the hypercube architecture is the Intel iPSC computer complex.
* It consists of 128(*n*=7) microcomputers, each node consists of a CPU, a floating-point processor, local memory, and serial communication interface units.



**Fig. 5.7: Hypercube structures for n=1,2,3**

# Multistage Switching Network